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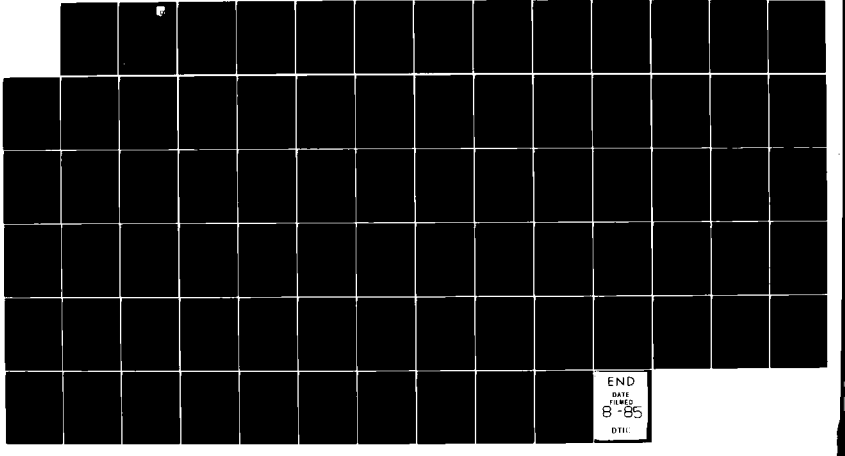

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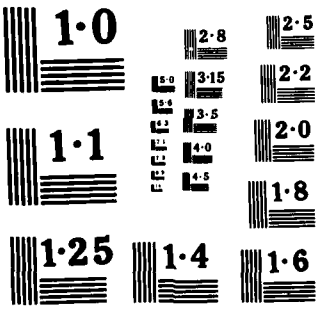
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MILLIMETER-WAVE CIRCUIT ANALYSIS AND SYNTHESIS

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May 1985

Final Report for Period March 1981-April 1985

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This final report is a brief description of the work carried out under this program. In addition to the work reported here, several technical reports and journal articles were issued which describe the work performed in much greater detail. These reports and articles are available. The work carried out under this program included the following: IMPATT device modeling and prediction of Si, GaAs and InP IMPATT performance at millimeter wavelengths and their optimum design; modeling and characterization of GaAs MESFETs and

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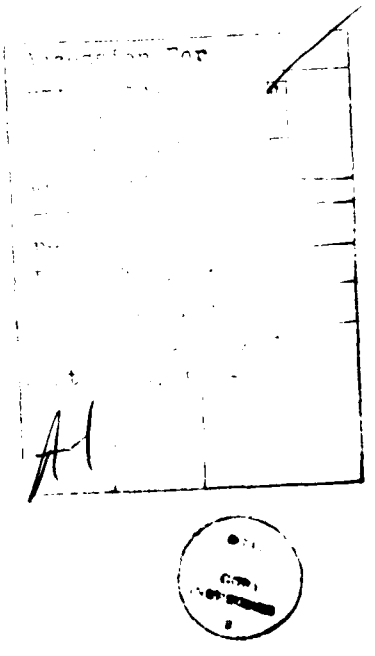
ABSTRACT CONT.

measurement of small- and large-signal equivalent circuit parameters; design and fabrication of a monolithic GaAs integrated circuit FET-varactor doubler; and analysis and design of a YIG loaded waveguide for magnetostatic device applications, such as tunable delay lines.

FOREWORD

This report describes the work carried out in the Solid-State Electronics Laboratory, Department of Electrical Engineering and Computer Science, The University of Michigan, Ann Arbor, Michigan, on "Millimeter-Wave Circuit Analysis and Synthesis." This work was sponsored by the Air Force Systems Command, Avionics Laboratory, Wright-Patterson Air Force Base, Ohio, under Contract No. F33615-81-K-1429 (Project 2002, Task 03, Work Unit 92).

The work reported herein was performed during the period March 1, 1981 to April 30, 1985 by Drs. G. I. Haddad, D. F. Peterson, R. K. Mains, and M. E. Elta and Messrs. R. Actis, T. L. Crandle, J. R. East, R. K. Froelich, M. Radmanesh, P. A. Sanborn, and D. Yang. The report was released by the authors in April 1985.



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SECTION I

INTRODUCTION

The purpose of this program was to investigate various types of microwave and millimeter-wave devices and circuits and device-circuit interactions in order to advance the state of the art and understanding of these devices and circuits and their utilization in optimizing the performance of oscillators, amplifiers, power combiners and in other applications.

Several areas of investigation were carried out and included, in most instances, device modeling, device characterization, circuit design and evaluation, and device-circuit interactions. The major areas that were studied under this program and the important results that were obtained are summarized in the following sections of this report and include the following:

1. IMPATT device design and optimization.
2. Power combining of solid-state devices.
3. FET device and circuit modeling and characterization including monolithic GaAs integrated circuits.
4. Magnetostatic-wave device design and analysis.

Several interim technical reports, journal articles, and conference paper presentations, which describe in detail various aspects of the work performed under this program, were issued and are available. These include:

A. Technical Reports

1. Froelich, R. K., "Computer Modeling of Millimeter-Wave IMPATT Diodes," Report No. AFWAL-TR-82-1107, November 1982.

2. Mains, R. K. and Haddad, G. I., "Capabilities and Potential of Millimeter-Wave IMPATT Devices," Report No. AFWAL-TR-82-1141, November 1982.

3. Yang, D. C., "Large-Signal Characterization of Nonlinear Two-Port Active Networks," Report No. AFWAL-TR-84-1034, April 1984.

4. Actis, R., "Lossless Symmetric TEM Line IMPATT Diode Power Combiners," Report No. AFWAL-TR-84-1035, April 1984.

5. Radmanesh, M., "Magnetostatic-Wave Propagation in a Finite YIG-Loaded Rectangular Waveguide," Report No. AFWAL-TR-84-1174, November 1984.

6. Peck, D. E., "Measurement Methods for Accurate Microwave Characterization and Modeling of MESFET Chips," Report No. AFWAL-TR-84-1177, January 1985.

B. Journal Articles

1. Blakey, P. A. and Froelich, R. K., "On the Transient Analysis of Circuits Containing Multiple Diodes," IEEE Trans. on Microwave Theory and Techniques, vol. MTT-31, No. 9, pp. 781-783, September 1983.

2. Mains, R. K., Haddad, G. I. and Blakey, P. A., "Simulation of GaAs IMPATT Diodes Including Energy and Velocity Transport Equations," IEEE Trans. on Electron Devices, vol. ED-30, No. 10, pp. 1327-1338, October 1983.

3. Mains, R. K., El-Gabaly, M. A., Haddad, G. I. and Sun, J. P., "Comparison of Theoretical and Experimental Results for Millimeter-Wave GaAs IMPATT's," IEEE Trans. on Electron Devices, vol. ED-31, No. 9, pp. 1273-1279, September 1984.

4. El-Gabaly, M. A., Mains, R. K. and Haddad, G. I., "Effect of Doping Profile Variation on GaAs Hybrid and Double-Read IMPATT Diode Performance at 60 and 94 GHz," IEEE Trans. on Microwave Theory and Techniques, vol. MTT-32, No. 10, pp. 1348-1352, October 1984.

5. El-Gabaly, M. A., Mains, R. K. and Haddad, G. I., "Effects of Doping Profile on GaAs Double-Drift IMPATT Diodes at 33 and 44 GHz Using the Energy-Momentum Transport Model," IEEE Trans. on Microwave Theory and Techniques, vol. MTT-32, No. 10, pp. 1353-1361, October 1984.

6. Mains, R. K., El-Gabaly, M. A. and Haddad, G. I., "Finite-Difference Numerical Methods for Solving the Energy-Momentum Transport Equations in Two-Valley Semiconductors," J. Computational Phys. (accepted for publication).

C. Conference Presentations

1. Yang, D. C. and Peterson, D. F., "Large-Signal Characterization of Two-Port Nonlinear Active Networks," 1982 IEEE MTT-S Int. Microwave Symp., Dallas, TX, June 1982. Also in Proc. pp. 345-347.

2. Mains, R. and Haddad, G. I., "Simulation of GaAs IMPATT Diodes Including Energy and Velocity Transport Equations," 1983 Workshop on Compound Semiconductors for Microwave Materials and Devices (WOCSEMMAD), San Antonio, TX, February 1983.

3. Actis, R. and Peterson, D. F., "A Lossless Radially Symmetric TEM-Line IMPATT-Diode Power Combiner," 1983 IEEE/MTT-S Int. Microwave Symp., Boston, MA, May 31-June 3, 1983. Also in Proc. pp. 209-211.

As can be seen from this list, significant contributions have been made in device and circuit design, characterization, and optimization. The following sections describe in more detail the results obtained under this program in the various areas.

increased understanding of the device.[4-9] However, the microwave FET structure poses a basic problem for the device modeler. An X-band FET has a typical doping density of 10^{17} cm^{-3}, with higher doping for higher frequency operation. The characteristic length in a semiconductor material is the debye length:

$$Ld = \left(\frac{2kT\varepsilon}{q^2 N_d}\right)^{1/2} , \qquad (1)$$

where k = the Boltzmann constant,

T = the temperature,

ε = the dielectric constant,

q = the electronic charge and

N_d = the doping.

The characteristic time is the dielectric relaxation time:

$$T = \frac{\varepsilon}{\mu q N_d} , \qquad (2)$$

where μ = the mobility.

The debye length is approximately 0.02 μm and the dielectric relaxation time is approximately 0.01 ps for an X-band FET. The problem with device modeling in two dimensions is constrained by the small mesh size and the resulting large number of calculations. The FET or switching problem means doing a solution approximately 100 times per picosecond. Through various approximations and clever programming the number of calculations can be reduced to some extent.

4.2.1 Simple Approximate Model. The approach used in this case is to derive a "quasi-two-dimensional" solution. The Poisson and electron transport equations, altered to account for the

SECTION IV

FET DEVICE AND CIRCUIT MODELING AND CHARACTERIZATION

4.1 Introduction. The purpose of this phase of the program was to develop appropriate theoretical models for GaAs FET transistors, to develop measurement techniques for experimental evaluation of the devices and comparison with the models, the utilization of these models in voltage-controlled oscillator design and implementation, and the development of monolithic integrated circuits incorporating these devices.

The results obtained on the various aspects of this phase of the program are summarized in the following sections.

4.2 FET Modeling. Several types of models were developed that range from simplified ones that lend themselves easily to analytic solution to very extensive two-dimensional computer models that require significant computer time for simulation.

During the past decade the FET has become the single most important microwave solid-state device. It is used in small- and large-signal amplifiers, low-noise amplifiers, oscillators, mixers, and a variety of control applications. The FET has been the subject of numerous papers leading to a better understanding of its operation and potential. Early FET models were analytic approximations that neglected the effect of space charge in the channel.[1-3] With faster computers and better numerical methods, full solutions of the two-dimensional carrier transport and Poisson's equations became possible. Results from these finite-difference and finite-element solutions

N-way nonresonant combiners which are often associated with various bandlimiting resistive stabilization techniques for suppressing non-power-producing interactions among the devices. This combining design requires no such stabilizing scheme. Suppression of undesired odd modes is accomplished in lossless circuits by an appropriate combination of device and circuit which provides the necessary condition for a stable combiner.

"An experimental realization of the simplest example of a lossless symmetric combiner design is presented in two different circuit mediums. A two-diode microstrip combiner and a two-diode coaxial combiner were developed to demonstrate the design principles. The combiners operated in a stable nonspurious amplifier configuration. A 3-dB bandwidth of 16 percent with 4.2 dB of gain was observed in the coaxial combiner with 94 percent combining efficiency."

SECTION III

POWER COMBINING OF SOLID-STATE DEVICES

3.1 Introduction. The purpose of this phase of the program was to investigate the properties of a new scheme for circuit-level power combining of negative-resistance devices. Both theoretical and experimental work was carried out in order to characterize such a scheme and to determine its potential. The new approach utilizes the properties of symmetric lossless TEM line combining networks, together with the bandlimited negative-resistance properties of two-terminal devices, to achieve stable combiner designs having improved bandwidths over other approaches. IMPATT devices were employed in an experimental realization and evaluation of this scheme.

3.2 IMPATT Diode Power Combining. The preceding scheme was employed in an IMPATT diode power combiner and the results obtained are given in detail in Technical Report No. AFWAL-TR-84-1035 entitled "Lossless Symmetric TEM Line IMPATT Diode Power Combiners," by P. Actis, April 1984. An abstract from this report is included here for completeness.

"The results of an experimental investigation into a new approach to circuit-level power combining of negative-resistance devices are presented. The approach uses the properties of symmetric lossless TEM line combining networks together with the bandlimited characteristics of IMPATT diodes to achieve stable combiner designs having improved bandwidths over other approaches. The combining networks utilized in this investigation fall into the category of

equations. Results of large-signal simulations of GaAs IMPATTs using these numerical methods are presented and compared."

M. A. El-Gabaly, R. K. Mains and G. I. Haddad, IEEE Transactions on Microwave Theory and Techniques, October 1984.

"Doping profile parameters were varied in a computer optimization of hybrid and double-Read GaAs IMPATT diodes at 60 and 94 GHz. The energy-momentum transport model was used to simulate each structure. Optimum results for the various structures that were studied are presented and compared."

4. "Effects of Doping Profile on GaAs Double-Drift IMPATT Diodes at 33 and 44 GHz Using the Energy-Momentum Transport Model," by M. El-Gabaly, R. K. Mains and G. I. Haddad, IEEE Transactions on Microwave Theory and Techniques, October 1984.

"Experimentally determined doping profiles for double-Read GaAs IMPATT diodes operating at 33 and 44 GHz are used as starting points for a computer optimization. A computer simulation including energy and momentum relaxation effects was used to simulate these devices as the lengths of the drift regions and the integrated charge in the doping spikes were varied. The effects of these doping profile variations on diode performance are presented."

5. "Finite-Difference Numerical Methods for Solving the Energy-Momentum Transport Equations in Two-Valley Semiconductors," by R. K. Mains, M. A. El-Gabaly and G. I. Haddad, Journal of Computational Physics, accepted for publication.

"Two finite-difference methods for solving the energy-momentum transport equations for electrons in two-valley semiconductors are analyzed. For each method, stability analyses are carried out including the electric field terms and relaxation terms in the

articles are included here for completeness.

1. "Simulation of GaAs IMPATT Diodes Including Energy and Velocity Transport Equations," by R. K. Mains, G. I. Haddad and P. A. Blakey, IEEE Transactions on Electron Devices, October 1983.

"Simulations have been performed of GaAs hybrid double-drift IMPATT diodes at 60 and 94 GHz using a transport model which includes equations for the average per-carrier velocity and energy. These equations are obtained from the second and third velocity moments of the Boltzmann transport equations, respectively. The relaxation-time formulation is used to characterize the collision terms. Simulations were also carried out for the same structures using the standard drift-diffusion transport model. It was found that inclusion of the energy-velocity equations significantly modifies the predicted carrier transport behavior and results in somewhat better RF performance under large-signal conditions than that predicted by the drift-diffusion simulation."

2. "Comparison of Theoretical and Experimental Results for Millimeter-Wave GaAs IMPATT's," by R. K. Mains, M. A. El-Gabaly, G. I. Haddad and J. P. Sun, IEEE Transactions on Electron Devices, September 1984.

"Simulations are performed of GaAs IMPATT diodes for which experimental results are available at 20, 33 and 44 GHz. At each frequency, simulations are performed using both the drift-diffusion approximation and the energy-momentum transport model. It is found that inclusion of energy and momentum relaxation effects yields better agreement with experiment."

3. "Effect of Doping Profile Variation on GaAs Hybrid and Double-Read IMPATT Diode Performance at 60 and 94 GHz," by

determine better designs for millimeter-wave IMPATTs and to predict the ultimate potential of these devices.

Several IMPATT structures were simulated using both the drift-diffusion and energy-momentum models. When the energy-momentum equations were included for millimeter-wave GaAs IMPATT simulation, primarily three effects were observed. First, the induced current waveforms were altered from those calculated using the drift-diffusion simulation due to velocity under- and overshoots. Second, an additional delay in the avalanche process due to energy relaxation was observed. Finally, the precollection process for precollection-mode devices is altered by the inclusion of energy and momentum relaxation effects.

To compare the simulation results with experiment, both models were used to simulate GaAs IMPATT diodes for which experimental results are available at 20, 33 and 44 GHz. It was found that results from the energy-momentum simulation agreed better with experimental results at these frequencies.

A series of studies was carried out to find the effect of varying several doping profile parameters on device performance at 33, 44, 60 and 94 GHz. Since good agreement had been obtained between available experimental data and the results of the energy-momentum simulation, this model was used in these studies. The overall goal was to predict optimum doping profiles for GaAs IMPATT diodes at these frequencies.

The methods employed in these simulations and the results obtained on millimeter-wave GaAs IMPATTs are given in detail in the following journal articles and the abstracts from these

"The model uses the first three velocity moments of the phase-space transport equation. Terms accounting for the effects of collisions incorporate energy dependent relaxation times and ionization rates. These functions of energy have been evaluated by requiring consistency with experimentally determined transport parameters. Stable, accurate and efficient finite-difference approximations to the transport equations were developed.

"The simulation was used to identify and examine the influence of various transient transport phenomena, including velocity overshoot and undershoot, and the lag of energy with respect to electric field. The most important effect was found to be the energy lag. This delays carrier injection, thereby improving predicted device performance.

"The results indicate that parasitics, rather than internal transport mechanisms, are dominant in determining the experimental performance attainable from millimeter-wave Si IMPATTs. The maximum frequency of operation of the IMPATT mode is subject to a fundamental limit associated with the energy relaxation time. This limit is approximately 500 GHz for Si IMPATTs."

The new model was next applied to GaAs diodes. Here there were three principal objectives. First, it was desired to know how the new effects included in the energy-momentum transport model would alter the device performance from that predicted by the drift-diffusion model. Second, the results of both simulations were compared to available experimental data in order to determine which could better explain experimental results. Finally, doping profile optimizations were carried out using the energy-momentum model to

modifications was to include a more realistic band structure than is typically assumed in Monte Carlo simulations. For consistency, this band structure must be used when the integration over final states is performed in the calculation of the scattering rates needed for the Monte Carlo simulation. Also, particle velocities and energies should be calculated using a more realistic band structure during the simulation.

A computer program was developed that numerically integrates the scattering rate matrix elements for all the important scattering mechanisms over an arbitrary band structure. The band structure for GaAs obtained using the pseudopotential method was then used to calculate a complete set of improved scattering rates for GaAs.

A new model was first employed to determine the properties of Si IMPATT devices at millimeter wavelengths. It was found that, since the relaxation rates in Si are very fast, there was very little difference in the results obtained from the two models up to approximately 200 GHz. It was therefore concluded that the drift-diffusion model is adequate for Si up to very high frequencies. The results on Si are described in detail in Technical Report No. AFWAL-TR-82-1107 entitled "Computer Modeling of Millimeter-Wave IMPATT Diodes," by R. K. Froelich, November 1982. An abstract from that report follows.

"A model of millimeter-wave Si IMPATTs has been developed which includes transient transport effects neglected in the conventional drift-diffusion model. The new model is based on principles of energy and momentum conservation.

less numerical diffusion than the other method. The problem with this method is that it becomes unstable in the limit of low electric field and low particle energy, so that it cannot be used for device simulation where these conditions occur. The alternative simulation uses a modified Lax numerical method (modified so that the particle continuity equations are conservative). The advantage of this method is that it remains stable in the limit of low field and low particle energy. To achieve this stability, the method introduces more numerical diffusion than the forward-time, upwind-drift method. However, it was found that proper choice of space and time steps can minimize the numerical diffusion of the modified Lax method to acceptable proportions.

Details of these investigations were included in a journal article. The article was submitted to the Journal of Computational Physics and has been accepted for publication.

During this program, the displaced Maxwellian method for calculating relaxation times was investigated extensively. Relaxation times were calculated for many different values of constants in the expressions for the scattering rate matrix elements. For each set of relaxation times, the transport equations were solved in the uniform, dc limit to determine whether a good fit to the static velocity-electric field characteristic could be obtained. For all the cases that were tried, it was not possible to obtain a good fit to the velocity-field characteristic at high electric fields. Therefore, the displaced Maxwellian approach was abandoned.

Instead, it was decided to modify the Monte Carlo program to be useful at high electric fields. One of the necessary

is 525°K. Matching each device to 1-Ω circuit resistance gives an estimate of maximum obtainable pulsed power. Finally, CW and pulsed performance for all structures and materials are compared over the entire frequency range simulated."

A very comprehensive computer model that includes energy and momentum relaxation effects was developed and applied to Si and GaAs IMPATT device simulation and design. Many different numerical techniques for solving the energy-momentum transport equations were investigated. These included both one-step methods, where the transport equations are solved only once at each time advancement, and two-step, Lax-Wendroff-type methods, where the equations are solved twice per time step advancement. The investigation consisted of two main phases. First, the numerical methods were analyzed to determine the range over which the method should be stable, whether the numerical method accurately models the actual equations, and whether the method conserves particle number, total momentum, and total energy. If a particular method was promising, it was implemented in a version of the energy-momentum IMPATT simulation. Simulations were then carried out to test the performance of the method in practice.

As a result of these investigations, two different versions of the energy-momentum simulation were developed. Both versions utilize one-step time advancement schemes since stability problems were encountered with the two-step methods. (Another disadvantage of the two-step methods is that they are more costly.) One numerical method is the forward-time, upwind-drift finite-difference method. This is the more accurate of the two methods and introduces

Both models were employed to determine the properties of millimeter-wave IMPATTs and, in particular, Si, GaAs and InP devices. It was determined that the drift-diffusion model is adequate for Si devices to very high frequencies, but for GaAs the second model is most appropriate.

A comparison of the results obtained from these models with available experimental results indicates good agreement. The results obtained on millimeter-wave IMPATTs are described next.

2.2 Properties and Capabilities of Millimeter-Wave IMPATTs. Several technical reports and journal articles were prepared describing the results obtained in detail. All of these publications are available and there is no need to repeat the details here. A brief summary is given, however, for completeness.

The drift-diffusion model was employed to determine the properties and capabilities of Si, GaAs, and InP IMPATTs at millimeter wavelengths and, in particular, at 30, 44, 60 and 94 GHz. The results are given in detail in Technical Report No. AFWAL-TR-82-1141 entitled "Capabilities and Potential of Millimeter-Wave IMPATT Devices," by R. K. Mains and G. I. Haddad, November 1982. The abstract from this report is included here.

"Theoretical investigations of IMPATT diodes are carried out at 30, 40, 60 and 94 GHz. GaAs, Si and InP diodes are simulated. Several single- and double-drift doping profiles are considered. Extensive results as a function of RF voltage amplitude and dc current density are presented. Taking thermal resistance into account, the expected CW performance of each structure is presented, such that the maximum allowable diode temperature

SECTION II

IMPATT DEVICE DESIGN AND OPTIMIZATION

2.1 Introduction. The objective of this phase of the program was to determine the potential and capabilities of IMPATT devices for both pulsed and CW operation at millimeter wavelengths and to determine the effects of material parameters and device doping profile on the expected performance of these devices. In order to achieve these objectives, theoretical models were developed and utilized for this purpose. These represent the best models available for IMPATT device simulations and can be divided into two main categories as follows:

1. The first model is the so-called "drift-diffusion" model. It incorporates the static velocity-electric field characteristics of electrons and holes, and the ionization rates are assumed to be instantaneous functions of electric field. Other than those, the model is fairly general and gives important information relative to device design.

2. The second model is the so-called "energy-momentum-relaxation" model where intervalley transfer time, energy and momentum relaxation effects, and ionization rates as instantaneous functions of energy rather than electric field are included. This model, therefore, takes into account velocity overshoot and undershoot effects which become very important in GaAs, particularly at millimeter wavelengths.

two-dimensional nature of the problem, are solved in one dimension. Several analytic expressions are used to determine the geometry of the channel. These approximations give a set of equations that can be solved rapidly. At the same time most of the two-dimensional device physics remains.

The quasi-two-dimensional model separates a two-dimensional FET structure into a gate depletion region and a conducting channel. The electron concentration, electric field, electron velocity, electron diffusion coefficient, and current density are assumed to depend only on the x position with no y dependence. This geometry and a volume element from under the gate region are shown in Fig. 1. In this two-dimensional volume element, Poisson's equation

$$\oint E \cdot \hat{n}\, dl = -\int \frac{q}{\varepsilon} (N - N_d)\, dv \qquad (3)$$

becomes (for unit width)

$$B_I E_I - B_{I+1} E_{I+1} = \frac{q}{\varepsilon} (N_I - N_d) \Delta x \frac{B_I + B_{I+1}}{2} , \qquad (4)$$

where E_I = the average electric field in the x-direction on the left boundary,

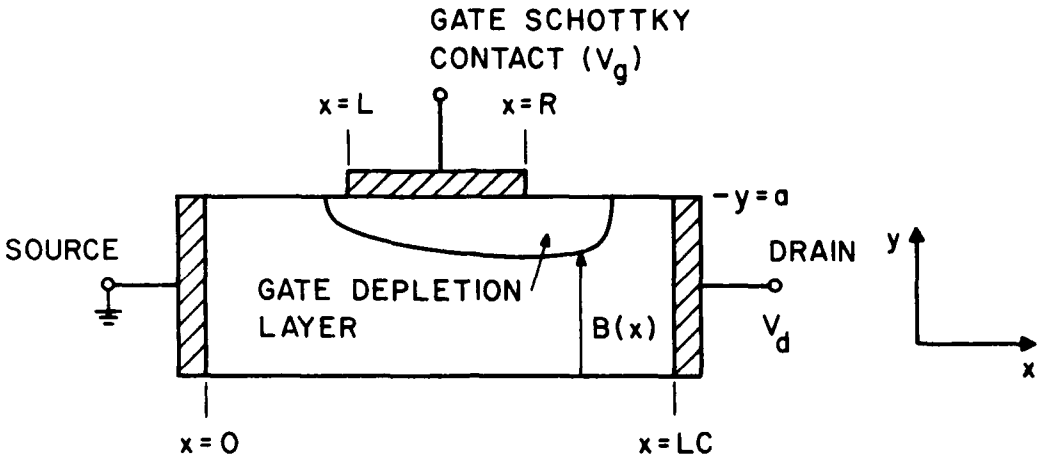
E_{I+1} = the average electric field in the x-direction on the right boundary,

N_I = the average electron concentration within the element,

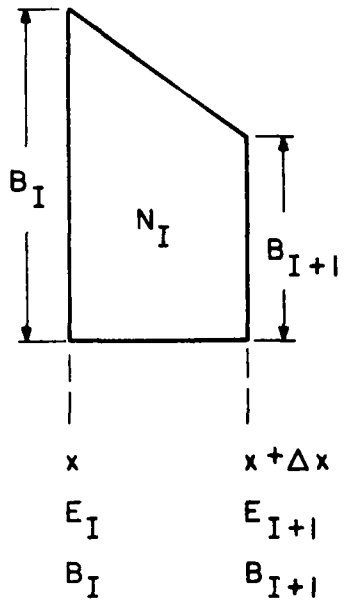
$\hat{n}$ = the unit normal vector and

N_d = the channel doping.

If a y-directed field were present, it would not change the results in Eq. 2. The y component would not cross the integration path of Eq. 1. In the limit of small Δx, Eq. 2 becomes



(a)



(b)

FIG. 1 (a) FET GEOMETRY AND NOTATION. (b) VOLUME ELEMENT GEOMETRY AND NOTATION.

$$\frac{\partial(BE)}{\partial x} = -\frac{q}{\epsilon}(N - N_d)B \quad . \tag{5}$$

The current continuity equation

$$\oint \vec{J} \cdot \hat{n}\, dn = \frac{\partial}{\partial t} \int N\, dv \tag{6}$$

can be written as

$$B_I J_I - B_{I+1} J_{I+1} = \frac{\partial}{\partial t}\left[N_I \left(\frac{B_{I+1} + B_I}{2}\right)\Delta x\right] \quad , \tag{7}$$

where $J_{I,I+1}$ = the electron current density at the left and right contacts. The electron current density is

$$J = Q\left[v(E)N(x) - D(E)\frac{dN(x)}{dx}\right] \quad . \tag{8}$$

In the limit of small Δx, Eq. 8 becomes

$$\frac{\partial(BJ)}{\partial x} = \frac{\partial(BN)}{\partial t} \quad . \tag{9}$$

Again, any y-directed current would not change the result of Eq. 9; however, a problem does exist. The velocity and diffusion coefficient in Eq. 8 depend on the total electric field, not just the x-directed component. At low fields the velocity depends linearly on the field and the diffusion coefficient is constant; however, at high fields the velocity is constant. The velocity along the channel depends on the angle of the electric field.[7] Equation 7 overestimates the current depending on the angle of the current in the channel. With this overestimate, the amount of charge in the channel dipole is usually correct within a few percent and the resulting drain-source terminal current is usually high by approximately 10 percent.

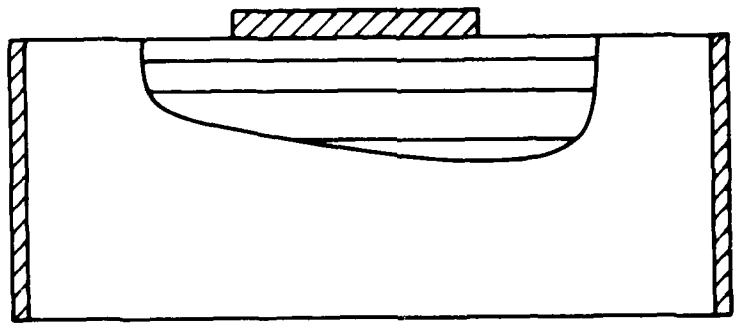
Before Eqs. 5 and 9 can be solved, an equation relating the voltage along the channel to the depletion layer width is needed. The voltage drop V_d across a depletion layer is related to its width w by

$$V_d = \left(\frac{q}{2\varepsilon}\right) N_d w^2 \qquad (10)$$

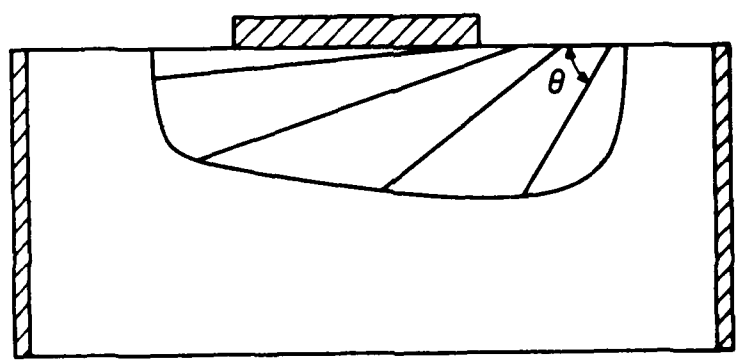
with V_d found by integrating across the width of the depletion layer along a suitable path. One possible approximation is to assume that the equipotential lines within the depletion layer are parallel to the gate as shown in Fig. 2. This approximation is typically used in analytic FET models and is correct in the limit of long gates.[1-3] With this approximation, the voltage drop across the depletion layer depends on the voltage difference between the channel and the gate. Equation 10 can be used to find the depletion-layer width and the resulting channel geometry factor B(x).

The problem with this approximation is that it always overestimates the width of the gate depletion layer. This can be shown by referring to Fig. 3 (taken from a two-dimensional result).[5] Although the constant voltage lines in the channel are approximately parallel, they bunch together in the depletion layer near the drain end of the gate depletion layer. Thus a sloping straight-line approximation can be made for the equipotential lines within the gate depletion layer. The two geometries are shown in Fig. 2. The electric field lines in the sloping approximation are semicircles. The width of the depletion layer in this case is

$$w' = w \sin \theta/\theta \quad , \qquad (11)$$



(a)



(b)

FIG. 2 POSSIBLE DEPLETION-LAYER POTENTIAL LINES. (a) PARALLEL-EQUIPOTENTIAL LINES AND (b) SLOPING-EQUIPOTENTIAL LINES.

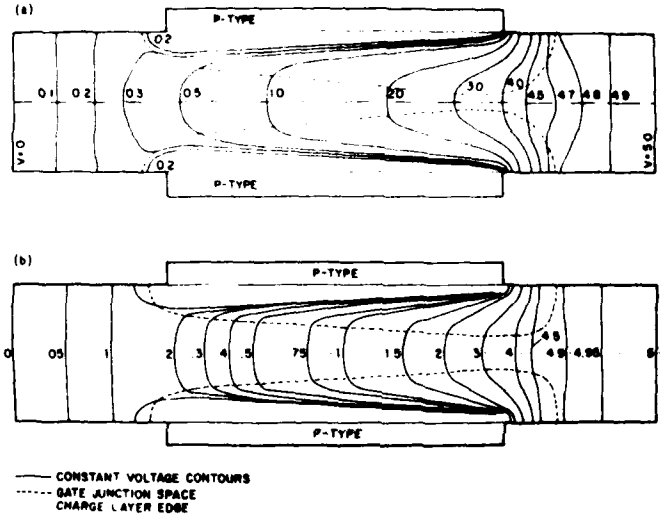


FIG. 3 CALCULATED VOLTAGE DISTRIBUTION IN A JFET. ($2w_g/w_c = 5.0$, $V_{sg} \approx 0$, $V_{sd} = 5.0$ V) (a) CONSTANT MOBILITY IN THE SOURCE-DRAIN CHANNEL. (b) FIELD-DEPENDENT MOBILITY IN THE SOURCE-DRAIN CHANNEL. (KENNEDY AND O'BRIEN[5])

where w = the depletion layer width from Eq. 10,

θ = the angle of the sloping equipotential line (shown in Fig. 3b) and

w' = the modified depletion-layer width.

For long gates $\theta \approx 0$ and Eq. 11 approaches Eq. 10. The effect of Eq. 11 compared to Eq. 10 is to reduce the depletion layer width for short devices. In the solution of the equations, both w' and θ depend on the voltage conditions along the channel. A Newton iteration is required at each space step to find the proper value of w'.

Equations 5 and 9, along with either Eq. 10 or 11, can be used to find the electron and field distribution along the channel of an FET if the geometry, material parameters, and bias conditions are specified. A computer program to solve these equations was written and a variety of structures were studied. The results for a typical Si and GaAs FET are presented and the dc results are used to describe small- and large-signal operation.

4.2.1a DC Results. The dc characteristics of a Si FET are shown in Figs. 3 and 4. The device has a channel doping of 10^{17} cm^{-3}, a channel height of 0.25 μm, a drain-source spacing of 0.5 μm and a 0.2-μm long gate. The FET quantities are all per centimeter of gate width. Figure 4a shows the drain-current vs. drain-source voltage for a range of gate voltages. Under dc conditions the channel of an FET is charge neutral with the channel dipole charge balanced and with the fixed doping charge in the depletion layer balanced by the corresponding image charge on the Schottky-barrier metal gate. Figure 4b shows the number of electrons on the gate. Increasing the gate voltage (more negative) increases the

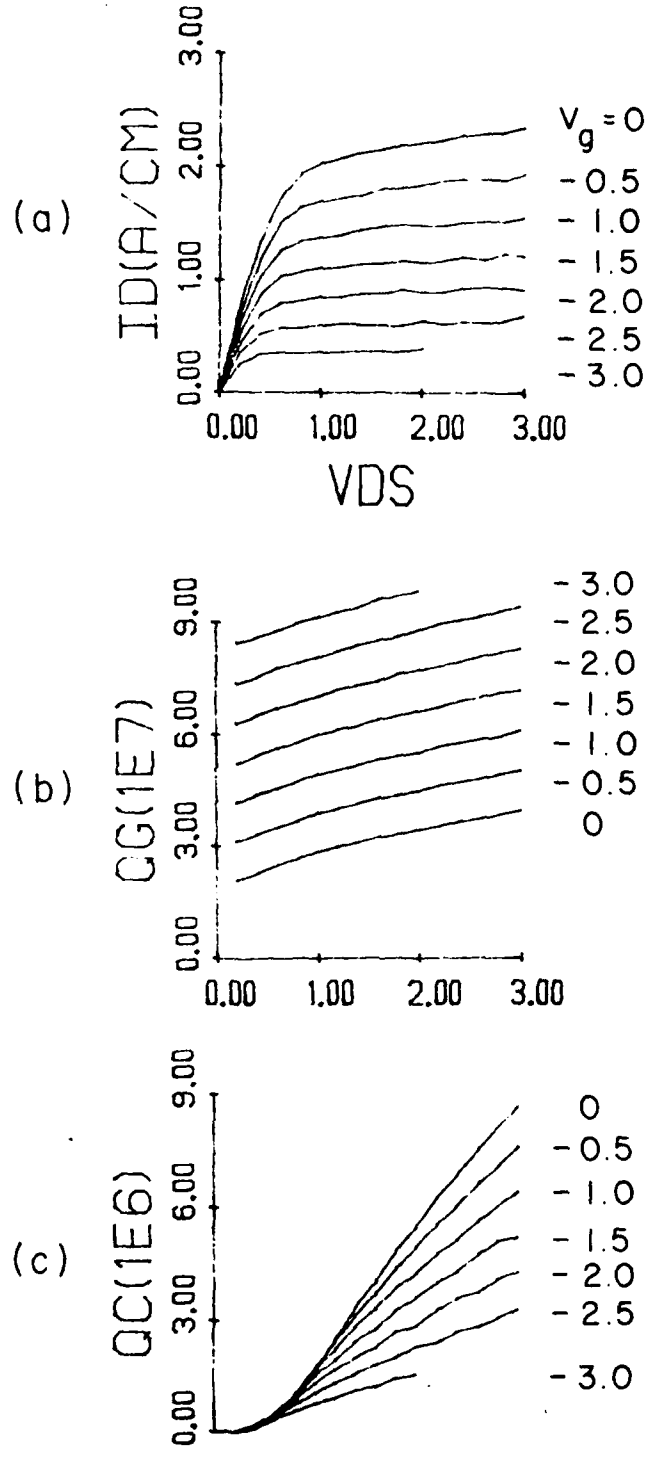


FIG. 4 Si FET PROPERTIES. (a) DRAIN CURRENT VS. DRAIN-SOURCE VOLTAGE, (b) GATE CHARGE VS. DRAIN-SOURCE VOLTAGE, AND (c) CHANNEL CHARGE VS. DRAIN-SOURCE VOLTAGE.

volume of the gate depletion layer. The volume and electron number also depend on the drain-source voltage as shown. The number of excess electrons in the accumulation layer of the channel charge dipole is shown in Fig. 4c. For low drain-source voltages the mobility is approximately constant and the channel dipole is small. Increasing the drain-source voltage increases the channel electric field and increases the number of electrons in the dipole accumulation region. Increasing the gate voltage (more negative) increases the volume of the gate depletion layer. Increasing the gate voltage (more negative) increases the size of the gate depletion layer which decreases the size of the channel dipole. Thus channel charge and gate charge go in opposite directions with gate voltage. The channel charge is approximately one tenth the gate charge.

The dc characteristics of a GaAs FET with the same geometry and doping as the previous Si device are shown in Fig. 5. Since the low field mobility in GaAs is approximately four times larger than in Si, the low drain-source voltage linear region resistance is also four times smaller. The GaAs device also reaches its peak velocity at a lower drain-source voltage. Further increasing the drain-source voltage drops the average electron velocity and the current. The gate charge is similar to the Si results with slight differences because of the voltage distribution along the channel and different material dielectric constants. The shape of the channel charge vs. drain-source voltage curve depends on the shape of the mobility vs. electric field curve. In Si the mobility is a monotonically decreasing function of field so the charge curves in Fig. 4c are smoothly increasing functions of field. In GaAs, the mobility is approximately

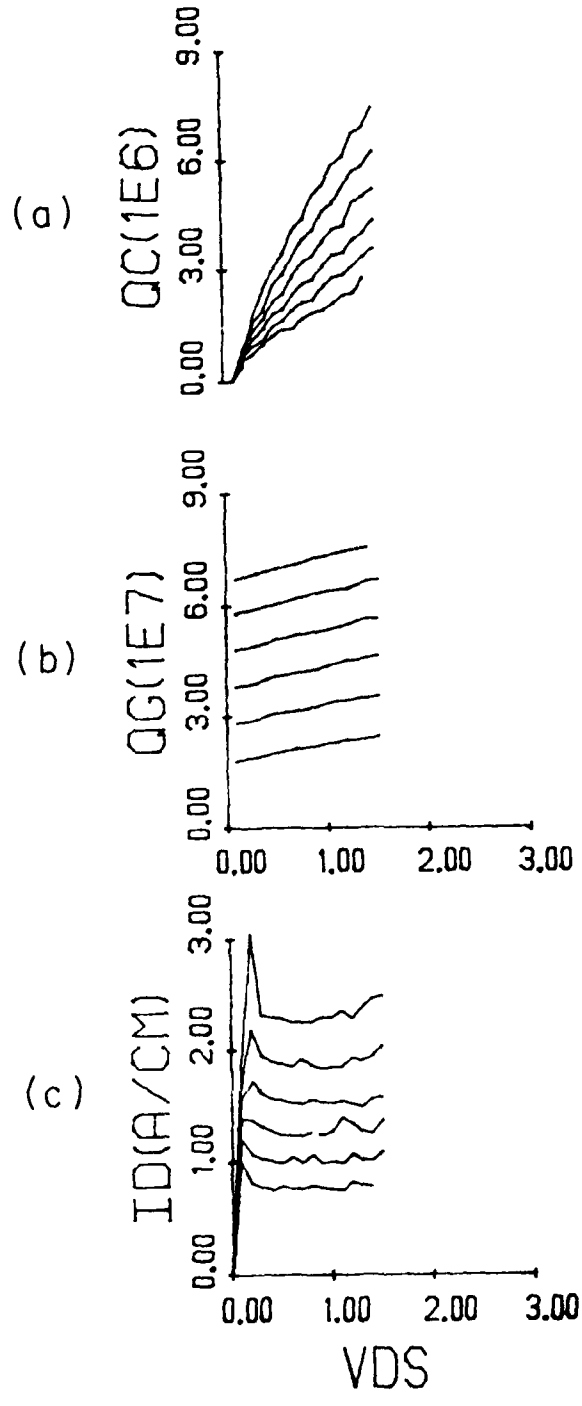


FIG. 5 GaAs FET PROPERTIES. (a) CHANNEL CHARGE VS. DRAIN-SOURCE VOLTAGE, (b) GATE CHARGE VS. DRAIN-SOURCE VOLTAGE, AND (c) DRAIN CURRENT VS. DRAIN-SOURCE VOLTAGE.

constant at low fields and drops rapidly for fields above the peak velocity field. In GaAs, the channel charge is approximately zero for peak channel fields below 3500 V/cm and then increases more rapidly than the Si case for larger fields or drain-source voltages.

The current, channel charge, and gate charge information shown in Figs. 4 and 5 were generated for a variety of FET structures. The information generated by the dc computer program is stored in tables and forms the basis of the small- and large-signal models discussed next.

4.2.1b Quasi-Static Charge Control Model. There are several possible approaches to describing small- and large-signal FET operation. The first approach is to use measured data and an equivalent circuit to model the performance.[10] Small-signal data is fitted to an equivalent circuit in order to determine the desired small-signal parameters over a range of bias conditions. The small-signal equivalent circuit can then be used to predict large-signal performance and for circuit design. This method works well for transistor circuit design.[11]

A second approach is to derive a small-signal equivalent circuit using an analytic dc solution as discussed in References 1 through 4. An extension of this method is given by Madjar and Rosenbaum.[12] The experimental approach depends on using measured data that limits the method to existing devices and requires time-consuming measurements. The dc small-signal method is limited by the assumptions of the underlying dc model.

The model adopted here uses information from the dc computer program to define a small-signal equivalent circuit. Since the

underlying dc program uses fewer assumptions than the models of References 1 through 4 and 12, the small-signal model should also be better. Also, most of the small-signal parameters depend on measurable quantities, so the model can be used as a starting point for experimental measurements.

The charge-control model used is shown in Fig. 6. The Q_g and Q_c boxes are the charge stored in the gate region and in the channel region. I_c is the channel current (under dc conditions the channel current is equal to the drain current). The quantities Q_c, Q_g and I_c are found using the dc program. Under time-varying conditions, the gate current is

$$I_g(t) = \frac{dQ_g(V_g,V_d)}{dt} \tag{12}$$

and the drain current is

$$I_d(t) = \frac{dQ_c(V_g,V_d)}{dt} + I_c(V_g,V_d) \quad . \tag{13}$$

A small-signal equivalent circuit can be derived from the charge-control model by performing a small-signal expansion of Q_c, Q_g, and I_c. The small-signal expression for Q_c is

$$Q_c(t) = Q_{co} + \Delta Q_c\, e^{j\omega t} = Q_{co} + \frac{\partial Q_c}{\partial V_g}\Delta V_g e^{j\omega t} + \frac{\partial Q_c}{\partial V_d}\Delta V_d e^{j\omega t} \quad ,$$

where ΔQ_c = the small-signal channel charge,

ΔV_g = the small-signal gate voltage and

ΔV_d = the small-signal drain-source voltage.

Similarly,

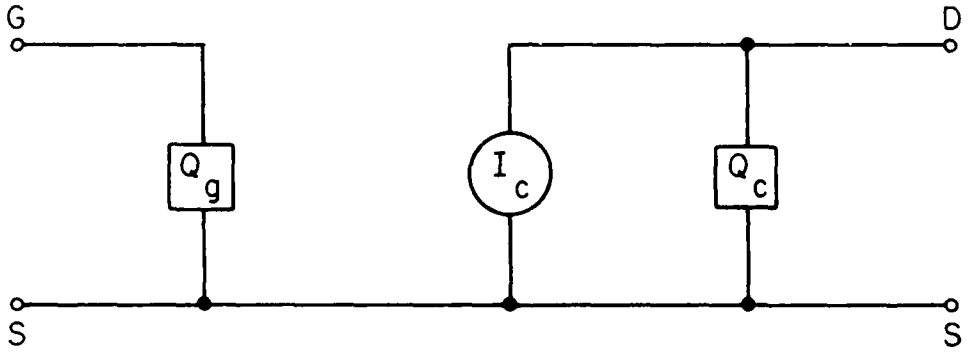


FIG. 6 CHARGE-CONTROL MODEL.

$$Q_g(t) = Q_{go} + \Delta Q_g e^{j\omega t} = Q_{go} + \frac{\partial Q_g}{\partial V_g} \Delta V_g e^{j\omega t} + \frac{\partial Q_g}{\partial V_d} \Delta V_d e^{j\omega t} \tag{15}$$

and

$$I_d(t) = I_{co} + \Delta I_d e^{j\omega t} = I_{do} + \frac{\partial I_d}{\partial V_g} \Delta V_g e^{j\omega t} + \frac{\partial I_d}{\partial V_d} \Delta V_d e^{j\omega t} , \tag{16}$$

where ΔQ_g = the small-signal gate charge and

ΔI_d = the small-signal channel current.

Using Eqs. 14 through 16 in Eqs. 12 and 13 yields

$$\Delta I_g(t) = j\omega C_g \Delta V_g + j\omega \tau_1 \Delta V_d \tag{17}$$

and

$$\Delta I_d(t) = g_m \Delta V_g + g_o \Delta V_d + j\omega \tau_2 \Delta V_g + j\omega C_o \Delta V_d , \tag{18}$$

where

$$C_g = \frac{\partial Q_g}{\partial V_g} = \text{the gate capacitance} ,$$

$$\tau_1 = \frac{\partial Q_g}{\partial V_d} ,$$

$$g_m = \frac{\partial I_d}{\partial V_g} = \text{the transconductance} ,$$

$$g_o = \frac{\partial I_d}{\partial V_d} = \text{the output conductance} ,$$

$$\tau_2 = \frac{\partial Q_c}{\partial V_g}$$

and

$$C_o = \frac{\partial Q_c}{\partial V_d} = \text{the output capacitance} .$$

this circuit was developed[15] but is reconsidered briefly to the extent that it relates to the calculations presented here.

The operation of the harmonic combiner relies on the matching of two active devices that are coupled through a physically symmetric network into a load. For this case, the y matrix for the matching network and load is of the form:

$$\begin{bmatrix} Y_{11} & Y_{12} \\ Y_{12} & Y_{11} \end{bmatrix} . \qquad (22)$$

If identical sources are then applied at the inputs of this two port, the eigenvectors and eigenvalues of the system are given by:

$$\mu_{m_k} = (\mu_m)^k = \begin{bmatrix} 1 \\ e^{jkma} \end{bmatrix} = \begin{bmatrix} 1 \\ -1 \end{bmatrix} \quad k = 1 \quad m = 1 ,$$

$$\begin{bmatrix} 1 \\ 1 \end{bmatrix} \quad k = 2 \quad m = 1$$

where k = the frequency multiple,

$$a = 2\pi/N$$

and N is the number of identical ports being combined. It is apparent that, for equivalent sources, the voltage on the load for the mode where m = 1 is restricted to second harmonic if higher-order components are neglected. The fundamental components from the two ports effectively cancel one another. By properly designing the matching network, the oscillation of the circuit can be confined to this mode only. Since for most cases the higher-order modes are negligible, the load absorbs only second-harmonic power. The matching which this circuit requires is ideally obtained by

"A large-signal equivalent circuit model of the MESFET is presented. This model can be established without extensive measurements and provides useful information in designing MESFET circuits for large-signal applications."

4.4 GaAs Integrated Circuits.

4.4.1 Introduction. This phase of the program was directed toward the study and fabrication of monolithic GaAs integrated circuits and, in particular, a symmetric second-harmonic power combiner. This circuit, which has yet to be implemented monolithically, has a tremendous potential for extending the power frequency limitations of a variety of active devices. The goals of this work were the fabrication of this circuit along with the development of an appropriate analysis to allow for the optimization of circuit performance and the extrapolation of these techniques to future circuits of this type.

The results persented here describe three facets of monolithic [illegible] circuit fabrication as well as some general characteristics of this class of circuits. A brief discussion of the characteristics of the circuit under consideration is presented in the next section. We shall now following describe three areas that have been developed in the course of this work: the fabrication of GaAs MESFETs and some measured characteristics of these devices, a simulation that was developed to determine the harmonic generation efficiency of a new varactor diode structure, and a processing schedule that makes these new device structures compatible for monolithic fabrication.

4.4.2 Circuit Description and Considerations. The circuit toward which this segment of the project is directed is a symmetric frequency doubler and power combiner. The theoretical basis for

from a model based on dc and low-frequency parametric measurements at the device terminals."

A Technical Report No. AFWAL-TR-84-1034 entitled "Large-Signal Characterization of Nonlinear Two-Port Active Networks," by D. C. Yang, April 1984. The abstract of the report follows.

"The objectives of this investigation include the development of a large-signal characterization procedure for nonlinear active two-port networks, analysis of the large-signal properties of MESFETs, and establishment of a large-signal MESFET equivalent circuit model.

"An approach for characterizing the single-frequency properties of a nonlinear two-port network is presented. The characterization results are useful in optimizing the external circuits for particular applications such as amplifiers and oscillators. The information obtained regarding network properties can be used for establishing amplifier and oscillator design and stability criteria.

"A GaAs MESFET was used as the nonlinear active two-port network, and its large-signal characteristics were measured. The nonlinear properties of the MESFET were investigated over the 7- to 13-GHz frequency range. The common drain configuration was studied extensively since this configuration is particularly advantageous for oscillator applications. The characterization results were applied to the design of common drain MESFET oscillators, and relationships between the output power and load impedances were established. The device performance as a voltage-controlled oscillator (VCO) was also investigated, with a single frequency oscillator built to verify the measurement results.

the program is described in great detail in the following technical reports and a brief description of the results is included here.

1. Technical Report No. AFWAL-TR-84-1177 entitled "Measurement Method for Accurate Microwave Characterization and Modeling of MESFET Chips," by D. E. Peck, January 1985. The abstract from this report follows.

"The subject of accurate measurement and modeling of three-terminal chip devices such as bipolar junction and field-effect transistors has been addressed by others with varying degrees of success. This paper discusses a two-tier approach for determining highly accurate wide-band scattering parameters of chip GaAs MESFETs that are referenced at the bonding pads of the device. In a two-tier approach the first level of characterization determines error corrections for a measurement system. The second level is characterization of any test fixture used in the measurement of the device. The discussion is directed at the second level of characterization in which methods of one-port untermination and deembedding are extended to two-port measurements and a technique known as 'cold chip' parasitic error correction is introduced which makes possible accurate placement of the S-parameter reference planes at the terminals on the chip device.

"Microwave modeling of the GaAs MESFET can be approached from two different directions, that of device physics and that of device measurements. This paper examines two different measurement-based modeling methods in which accurate chip level S-parameter data is a necessity. The first method uses the data directly to determine element values of an equivalent circuit model. In the second method the S-parameter data is used for comparsion to S-parameters predicted

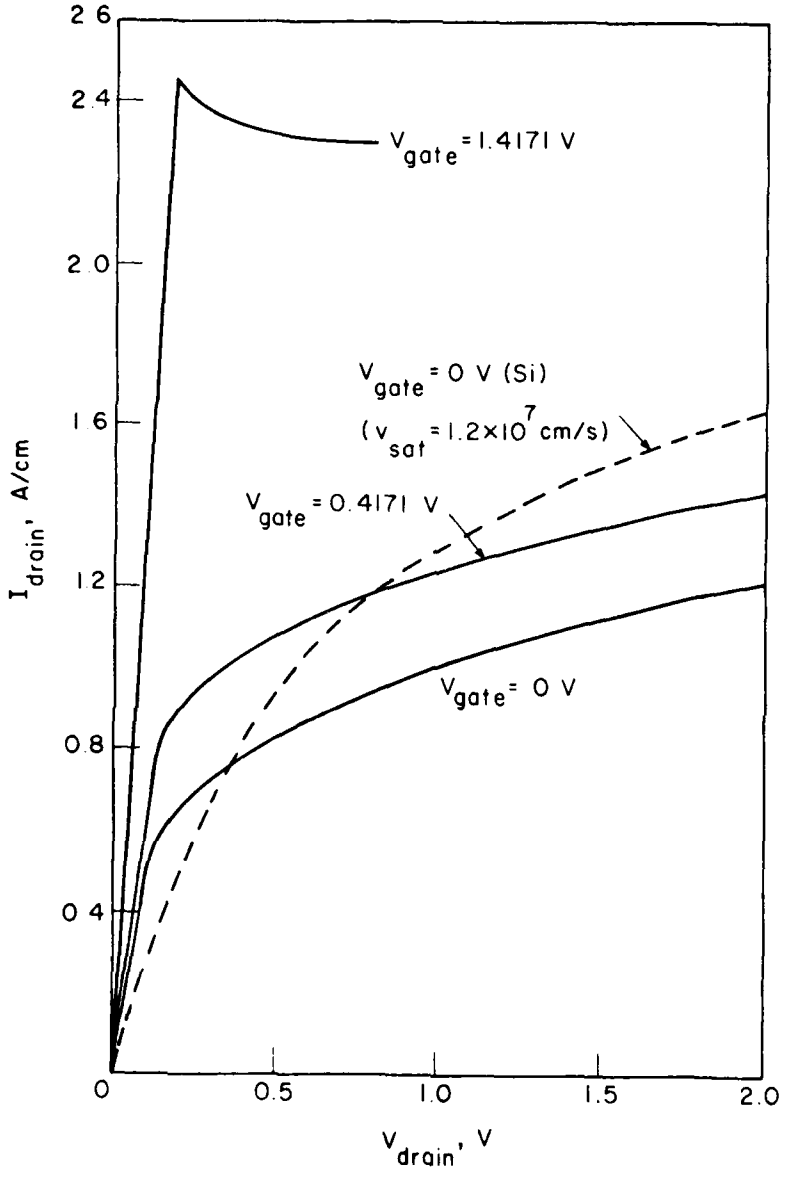


FIG. 12 I-V CHARACTERISTICS FOR CONVENTIONALLY DOPED GaAs FETs.

(v_{sat} = 8.0 x 10^6 cm/s and V_{bi} = - 1.4171 V)

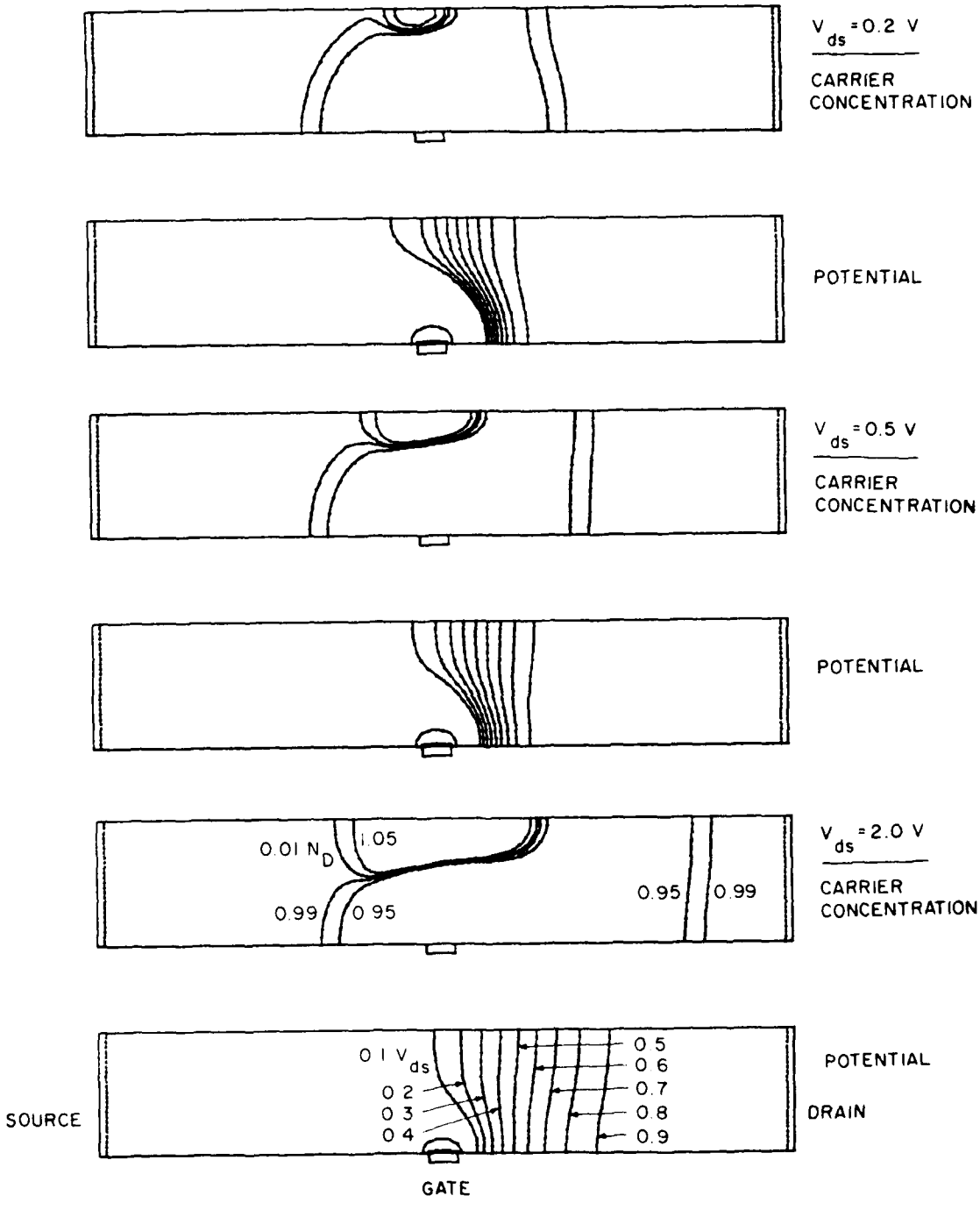


FIG. 11 GaAs CONVENTIONAL FET. (V_{gs} = 0.0 V, V_{bi} = - 1.4171 V, DOPING = 1.5 x 10^{17} cm^{-3}, DEVICE LENGTH = 0.68 μm, DEVICE WIDTH = 0.11 μm, AND GATE LENGTH = 0.035 μm)

more accurate method is required. Faricelli et al.[13] studied transient behavior using a two-dimensional transient analysis. Yang and Peterson[14] described the experimental large-signal characterization of FETs.

A simple and efficient dc and quasi-static RF model for FET operation was presented. This model includes much of the device physics neglected by simpler analytic models, while at the same time being much lower in cost than two-dimensional simulations. The model was used to predict the small-signal behavior of FETs. The model shows the importance of the channel dipole and the resulting effect on the transconductance. Quasi-static large-signal operation and the resulting limits were also discussed.

4.2.2 Computer Modeling of FET Devices. A two-dimensional drift-diffusion computer model was developed that can be applied to Si or GaAs devices. Typical results from this model for a GaAs FET are shown in Figs. 11 and 12. Because of the expense involved in using this model, it was not used extensively to simulate many devices. It was used, however, to compare with the approximate model described in the previous section and good agreement was obtained. The computer program was tested and appears to be working properly.

4.3 Experimental Characterization of GaAs FETs. Techniques were developed for experimental characterization of GaAs MESFETs and for measurement of small- and large-signal equivalent circuit parameters. This is extremely important for determining the properties of these devices and their utilization in amplifiers, oscillators, and in other applications. The work performed under this phase of

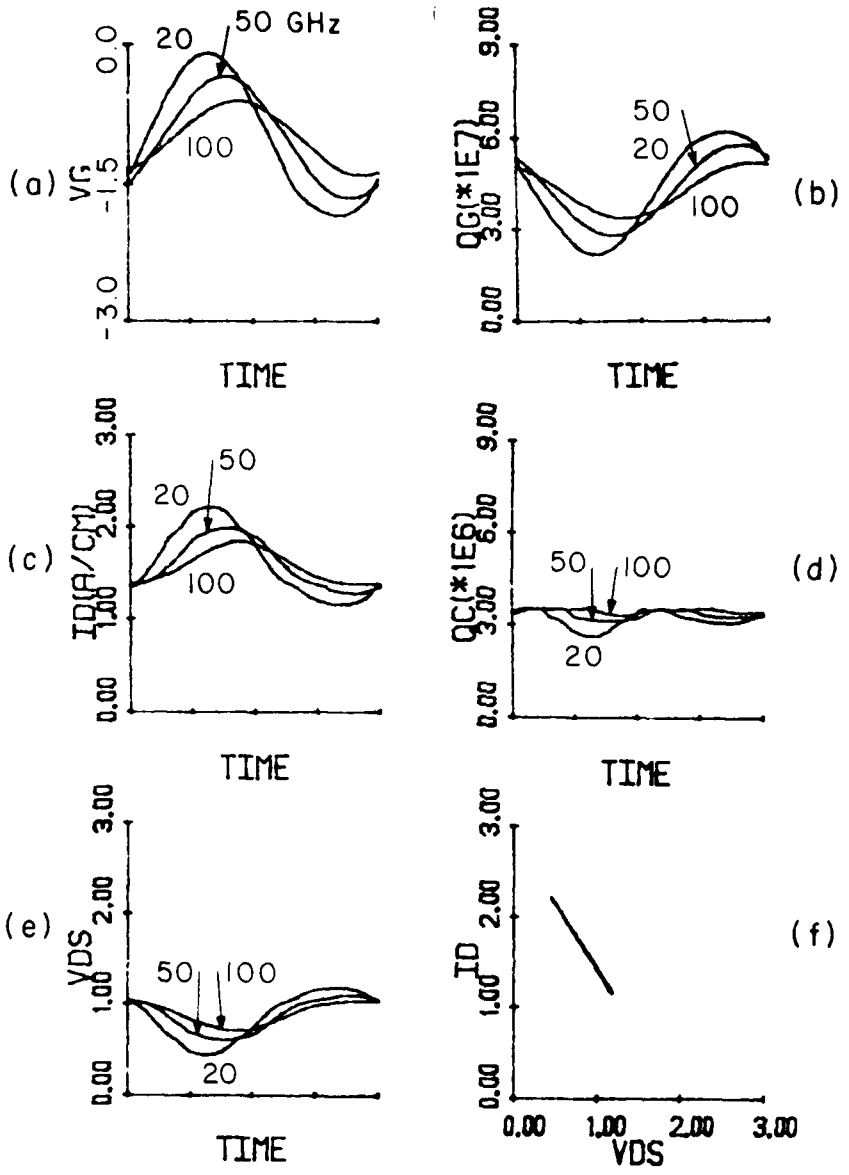


FIG. 10 LARGE-SIGNAL QUASI-STATIC OPERATION OF A GaAs FET.

time. The drain current vs. time is shifted with respect to the gate voltage by the τ_1 delay discussed previously. The delay time for this case is approximately 5 ps. The current is slightly clipped at higher gate reverse bias because of the transconductance reduction there. The channel charge vs. time is shown in Fig. 9d. Two effects acting together produce the double peak curve shown. The first peak corresponds to the minimum gate reverse bias and maximum channel dipole volume. The second peak occurs when the drain-source voltage is approaching a maximum, producing a larger electron density in the dipole. The drain-source voltage and operating load line are shown in Figs. 9e and 9f.

A set of curves for the GaAs device of Fig. 3 is shown in Fig. 10. For this example, R_g = 1 Ω, R_d = 0.7 Ω, and w = 2 V. The gate is biased with a - 1 V gate voltage and a 1 V RF voltage. The three sets of curves correspond to frequencies of 20, 50 and 100 GHz. The combination of R_g and the gate capacitance lowers the RF voltage across the gate terminal with increasing frequency. This, in turn, reduces the other quantities shown in Fig. 10.

The performance of the GaAs device is similar to that of the Si device, with small differences because of the shape of Q_c. This similarity points out the basic limitation of quasi-static models, or any model that derives large-signal information on the basis of small-signal calculations or measurements. The quasi-static model assumes that conditions in the channel are described by the stored charge and the channel current. However, depending on the bias point, RF voltage, and RF frequency, the channel conditions can be altered by the current flowing through the gate. Under these conditions a

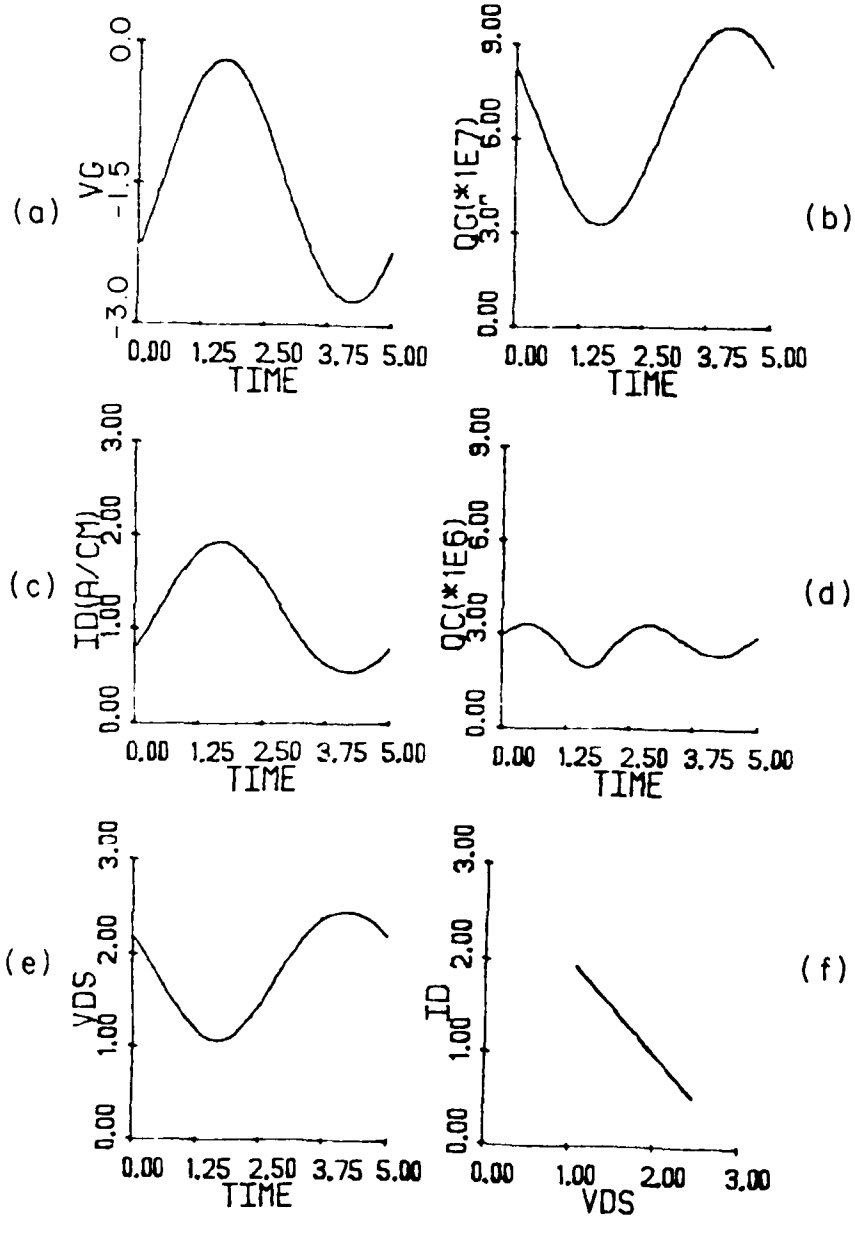


FIG. 9 LARGE-SIGNAL QUASI-STATIC OPERATION OF A SILICON FET.

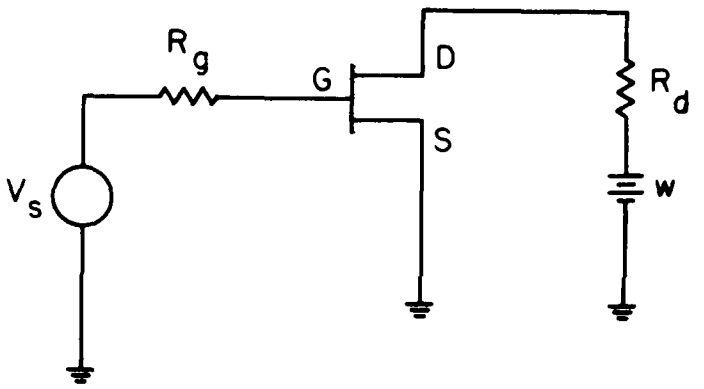


FIG. 8 QUASI-STATIC LARGE-SIGNAL CIRCUIT.

changes the amount of charge in the gate depletion layer, resulting in an additional gate current $j\omega\tau_1 \Delta V_d$.

The small-signal FET parameters depend on the dc operating point chosen. Typical small-signal parameters for the devices depend on the parameters in Figs. 4 and 5. This model is a model for the intrinsic FET. Additional elements would be required to describe parasitic losses and the effects of bondwires.

Equations 12 and 13 can also be used to describe large-signal quasi-static operation. Expanding the time derivatives in these two equations gives

$$I_g(t) = \frac{\partial Q_g}{\partial V_g} \frac{\partial V_g}{\partial t} + \frac{\partial Q_g}{\partial V_d} \frac{\partial V_d}{\partial t} \tag{20}$$

and

$$I_d(t) = \frac{\partial Q_c}{\partial V_g} \frac{\partial V_g}{\partial t} + \frac{\partial Q_c}{\partial V_d} \frac{\partial V_d}{\partial t} + I_c(V_g, V_d) \quad . \tag{21}$$

These equations, along with information on the circuits connected to the drain and gate, describe the large-signal operation under a variety of drive conditions.

A very simple bias circuit is shown in Fig. 8. The FET is biased with 1-Ω gate and drain resistance, a drain supply voltage of 3 V and a dc gate bias of - 1.5 V. Figure 9 shows the operation of a Si FET shown in Fig. 4 for a 1.5-V RF gate voltage at 25 GHz. The gate voltage is shown in Fig. 9a. The combination of R_g and the gate capacitance lowers the applied peak-to-peak voltage. The phase is also delayed. The corresponding number of gate electrons vs. time is shown in Fig. 9b. Figure 9c shows the drain current vs.

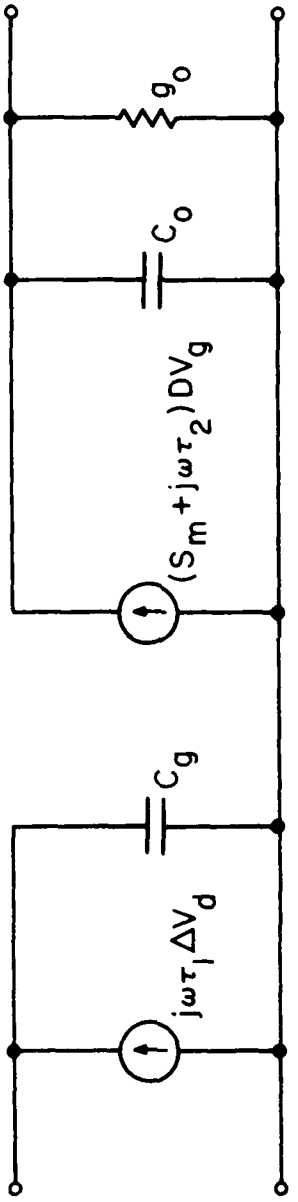


FIG. 7 SMALL-SIGNAL MODEL.

The small-signal equivalent circuit is shown in Fig. 7. The small-signal quantities are all found from the slopes of channel charge, gate charge, and channel current curves given in Figs. 4 and 5. C_{gs}, g_m and g_o are typical small-signal quantities. Most analytic models for FET operation neglect channel charge. However, the pumping of the channel charge by the drain-source voltage leads to an output capacitance.

The transconductance term in the equivalent circuit is modified by $j\omega\tau_2$. τ_2 corresponds to the charging and discharging of the channel charge dipole as the channel region volume is pumped by the gate depletion layer and gate voltage [$\tau_2 = (\partial Q_c/\partial V_g)$]. This charging and discharging produces an additional channel current $j\omega\tau_2$ lagging the normal current that is due to the combination of the transconductance and the gate voltage [lagging since τ_2 is a (-) quantity]. A typical equivalent circuit has a gate transit-time term $e^{-j\omega\tau}$ T to account for the measured phase delay of the drain current. For a small transit time the transconductance term becomes

$$g_{oe} - j\omega\tau_T \simeq g_o(1 - j\omega\tau_T) \quad . \tag{19}$$

The present equivalent circuit shows that the measured phase delay is also due to channel dipole conditions. τ_2 depends on the amount of charge in the channel dipole for various bias conditions. However, the characteristics of the charge dipole are approximately constant over a range of gate lengths, so τ_2 should not depend on gate length.

The feedback term τ_1 describes the coupling between the drain-source voltage and the gate charge. Changing the drain-source voltage

fabricating the entire circuit monolithically in a physically symmetric structure. The fabrication techniques that are described in the following sections have all been designed with this factor in mind.

4.4.3 Results. In the course of this investigation several tasks were performed and are discussed in the following order:

1. GaAs MESFET fabrication. A variety of processing techniques for the fabrication of GaAs MESFETs were explored. They were used to produce structures that were evaluated for dc and extrapolated for microwave performance. These show good performance and the results are presented here.

2. Varactor diode simulation and fabrication. Efficient harmonic generation requires a high degree of nonlinearity. A nearly lossless method for providing such a nonlinearity is provided by the varactor diode. Typically, the desired structure for these devices is a high-low-high doping profile. A new device structure that utilizes ion implantation to produce a vertical profile of this sort was simulated and showed excellent characteristics.

3. Monolithic fabrication. The fabrication of devices, such as MESFETs and varactors, monolithically requires a means of providing differing electrical characteristics on a single substrate. The method for implementing this is selective implantation into a semi-insulating substrate. This provides the required electrical characteristics with a minimum of process technicality and a great deal of design flexibility.

Each of these tasks is discussed in more detail in the following sections.

4.4.4 MESFET Fabrication. Table 1 gives a skeletal outline of the process used to fabricate the GaAs MESFETs that are discussed here as well as some characteristics of each processing step. Figures 13 through 15 show measured data from FETs fabricated on ion-implanted low-noise material. When the methodology described by Fukui[16] is used, the maximum available power can be determined in a straightforward manner from these plots. The gate capacitance vs. applied voltage curve given in Fig. 15 and the transconductance that can be determined readily from Fig. 13 make possible a simple calculation of the unity gain frequency. The FETs fabricated on this material showed good characteristics and typical unity gain frequencies of approximately 8 GHz. Maximum available power for typical devices on this material was also calculated and typical values of approximately 30 mW for 100-μm gate structures were obtained. A significant improvement in both power and frequency performance of these devices is expected for substrates with thicker more heavily doped active layers. The final design of the doubler circuit will necessarily include the consideration of the characteristics of the active channel and circuit considerations that limit circuit power consumption.

4.4.5 Varactor Modeling and Process Sequence. A nearly ideal method for generating harmonic power is provided by the varactor diode. The application of a sinusoidal voltage to this device gives a time variant capacitance that results in deviations from the purely sinusoidal current that would be obtained across a constant capacitance. To produce a large harmonic component it is generally desirable to maximize the variations in capacitance vs. time. The general characteristics that make for efficient harmonic

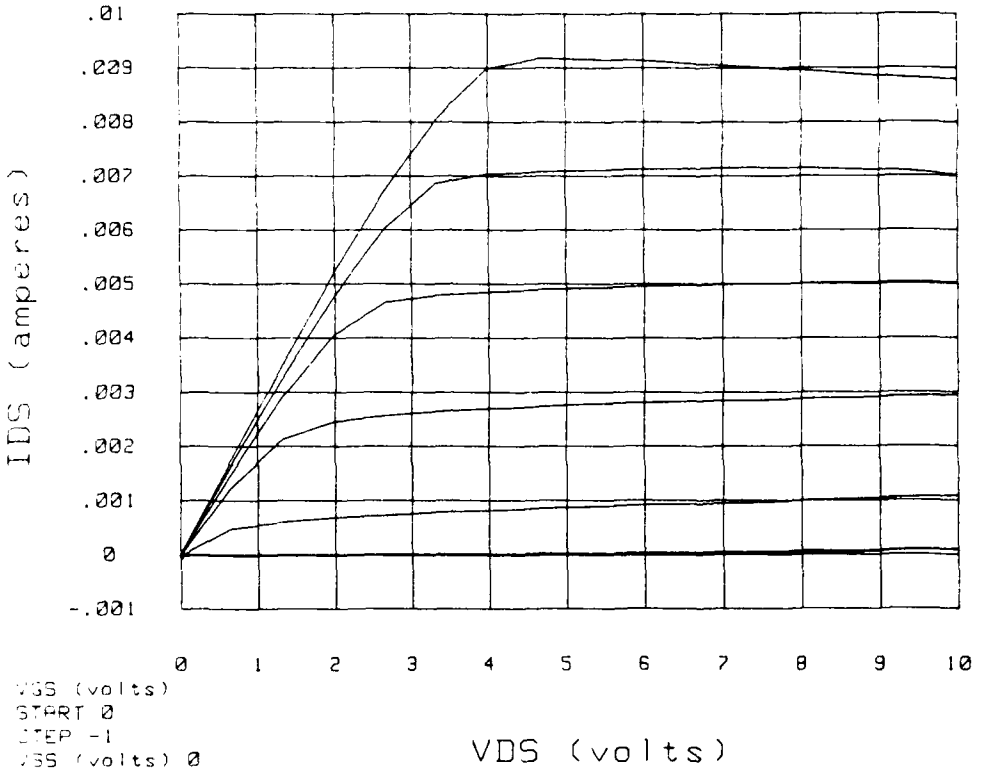


FIG. 13 TYPICAL MEASURED DRAIN I-V CHARACTERISTICS FOR LOW-NOISE FET.

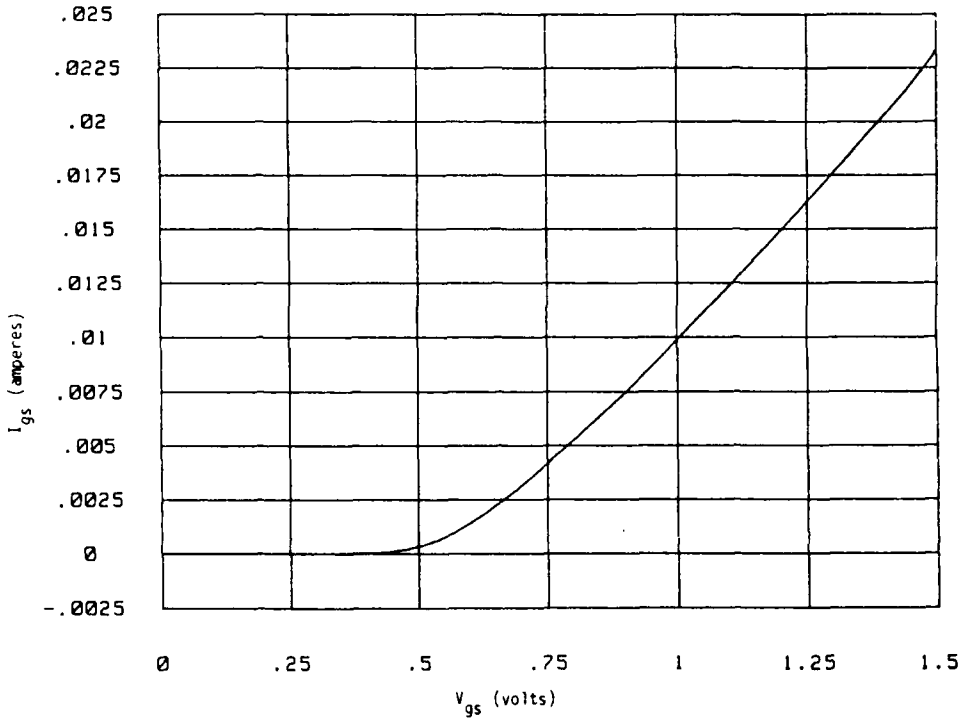


FIG. 14 I-V CHARACTERISTIC OF FORWARD-BIASED SCHOTTKY DIODE USED TO DETERMINE PARASITIC RESISTANCES (INCLUDES PARASITIC PROBE RESISTANCE).

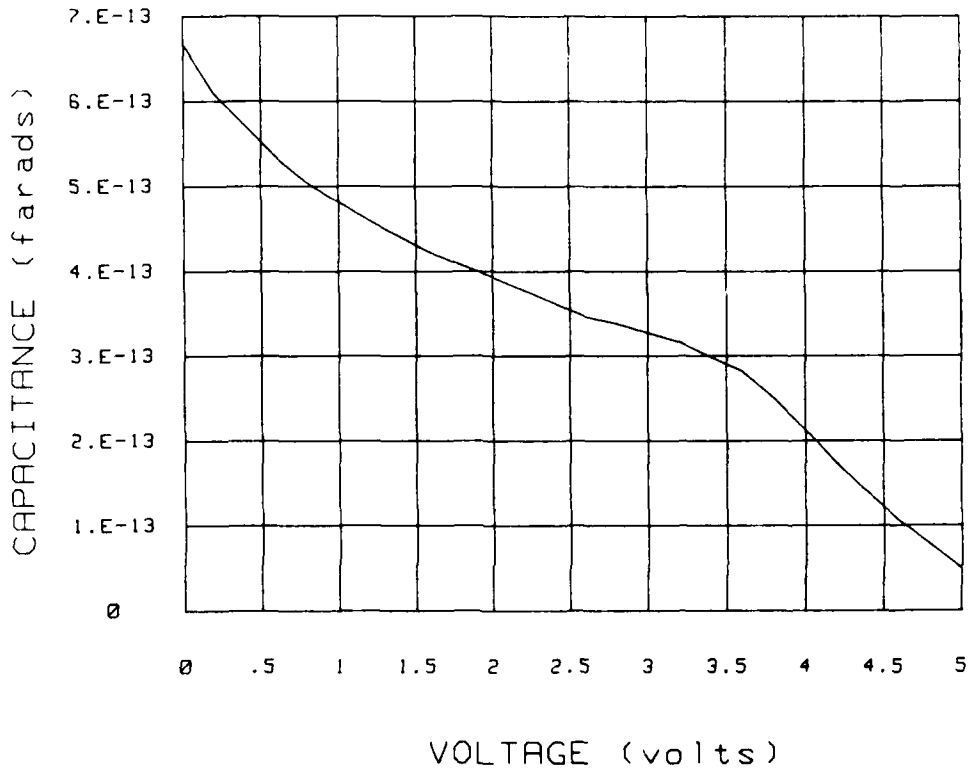


FIG. 15 CAPACITANCE-VOLTAGE PROFILE FOR TYPICAL SCHOTTKY DIODE ON LOW-NOISE MATERIAL.

generation can be pointed out by consideration of an unrealistic device that nonetheless brings out the salient features. This structure consists of an impulsive doping spike at the surface to which the Schottky contact is made. This causes the zero bias depletion width to approach zero and allow for a subsequently large variation in the capacitance that is inversely proportional to the depletion width. Beyond the zero bias depletion width it is optimal to have intrinsic material so that the variation in depletion width with respect to voltage is maximized. The depletion width as a function of voltage for this case is given by:

$$w \cong \left[\frac{2\varepsilon V}{qN_D}\right]^{1/2} , \tag{23}$$

where V is the reverse voltage and N_D is the doping density. Consequently, the variation of w with voltage is given by:

$$\frac{\partial w}{\partial V} = \left[\frac{\varepsilon}{2qN_D V}\right]^{1/2} . \tag{24}$$

It is readily apparent from this expression that the maximum variation in capacitance occurs at small reverse voltages and low dopings.

In practice, this type of structure is limited by a variety of considerations. These include:

1. The thickness of the barrier through which electrons must tunnel to contribute to current flow is controlled by the doping at the surface. In order to avoid a deleterious tunneling current it is necessary to reduce the doping at the surface.

2. The peak field in a varactor diode occurs at the interface between the metal and the semiconductor. If it is assumed that the

impulse of doping is replaced by a highly doped region, the field in the highly doped region is given as:

$$\tilde{E}(x) = E_{max}\left(1 - \frac{x}{w_o}\right) ,$$

where w_o = the zero bias depletion width = $\sqrt{2\varepsilon V_B/qN_D}$,

V_B = the barrier height and

$E_{max} = 2V_B/w_o$

at zero bias. If, as suggested by the discussion of the idealized structure, the zero bias depletion width extends across the highly doped region, the width and doping of this region will be the primary determinant of the breakdown voltage of the structure. It is desirable for power and tuning considerations that the breakdown voltage be maximized. It is, therefore, desirable to maximize the breakdown voltage and thus minimize the doping at the surface or at least extend the length of the highly doped region.

3. Parasitic resistance through the lowly doped region detracts from the overall efficiency of the device. This must be reduced by the introduction of a heavily doped buried layer as well as by increasing the doping of the intrinsic layer. It is important to note that the biggest variation in capacitance occurs as the depletion region varies around the zero bias condition. It is therefore more helpful to have a doping profile that increases toward the buried highly doped layer.

These considerations dictate that a criterion for evaluating varactors as harmonic generation sources must relate the relative importance of harmonic generating efficiency and resistive loss.

A straightforward analysis that results from the assumption that the varactor is excited by a sinusoidal voltage source gives a figure of merit for the varactor. For a given load, the loss of the varactor is proportional to

$$x = \frac{I_t^2 R_s}{I_2^2} ,$$

where I_t and I_2 are rms values of the total and first-harmonic current, respectively, and R_s is the series resistance of the varactor. This figure of merit is to be minimized for peak performance and can be used as a first-order comparison between two device structures. The general characteristics described previously are readily obtainable by a profile that uses the vertical doping profile of a properly designed ion implantation. An ion implant simulation based on the Pierson IV distribution was implemented. This was used to evaluate the capacitance vs. voltage and, consequently, the harmonic generating capability of a number of device structures. Fourier components of the current waveform were evaluated. In addition, the vertical resistivity through the lowly doped region and the sheet resistivity of the buried layer were evaluated so that the series resistance of a particular layout configuration could be determined. This makes a comparison of two device structures possible using the method described. Figures 16 and 17 show a typical implant profile and the associated capacitance-voltage characteristic. Figures 18 through 20 show an RF voltage and the response of this device structure to this voltage. The Fourier coefficients displayed on the plot show a good harmonic generating capability while maintaining a reasonably low parasitic resistance. The fabrication procedure for these devices is similar

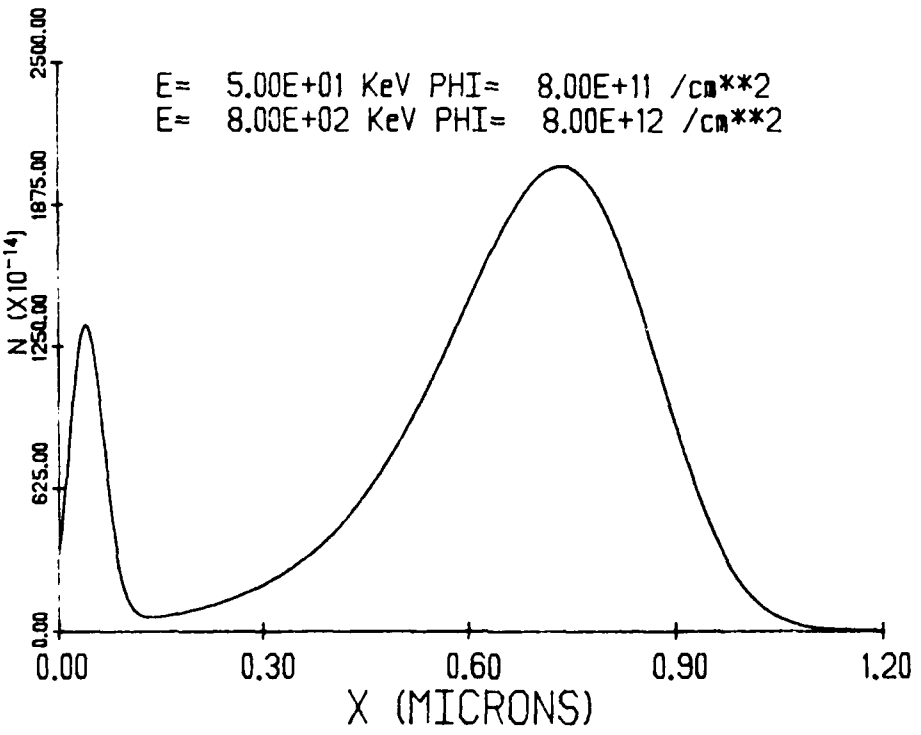


FIG. 16 IMPLANT PROFILE FOR ENHANCED HARMONIC GENERATION (Si INTO GaAs).

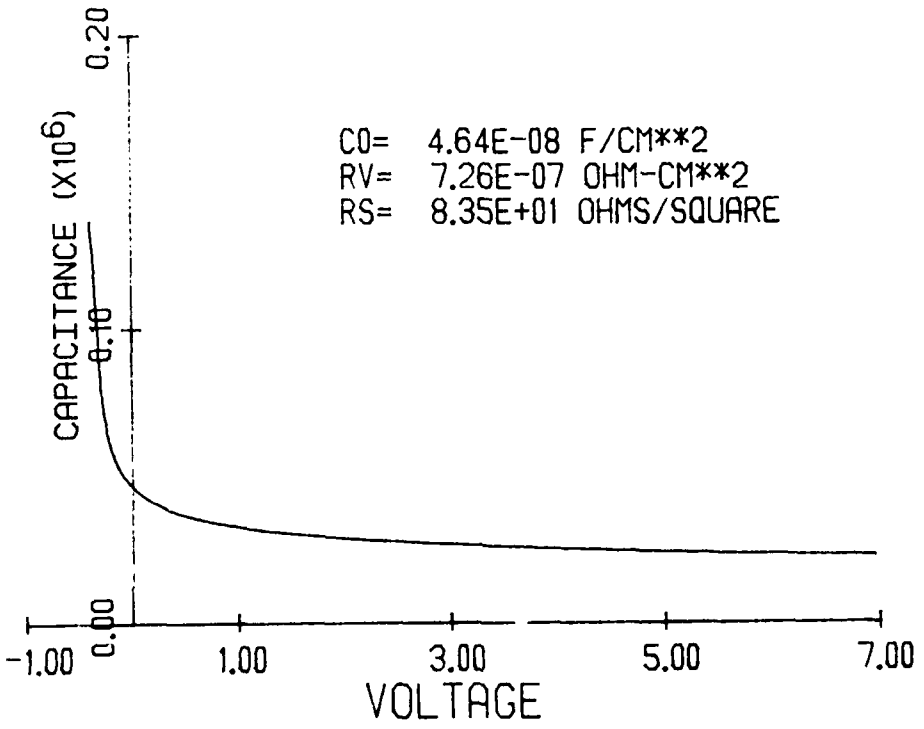


FIG. 17 CAPACITANCE-VOLTAGE CHARACTERISTIC FOR THE PROFILE OF FIG. 16. RV AND RS CAN BE USED TO CALCULATE THE PARASITIC RESISTANCE FOR A GIVEN LAYOUT CONFIGURATION.

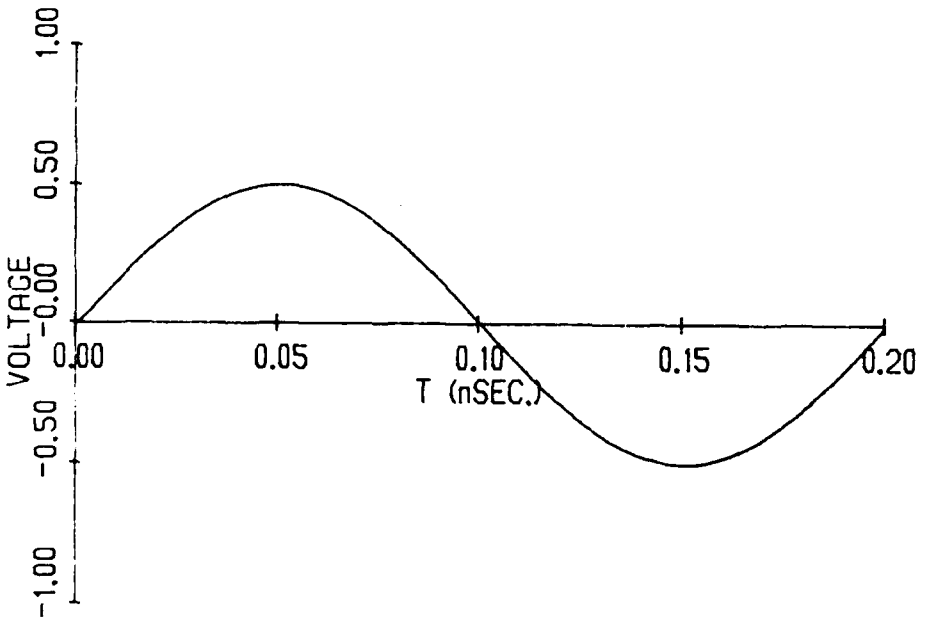


FIG. 18 APPLIED RF SIGNAL VOLTAGE AT 5 GHz (POSITIVE VOLTAGE REFLECTS REVERSE BIAS).

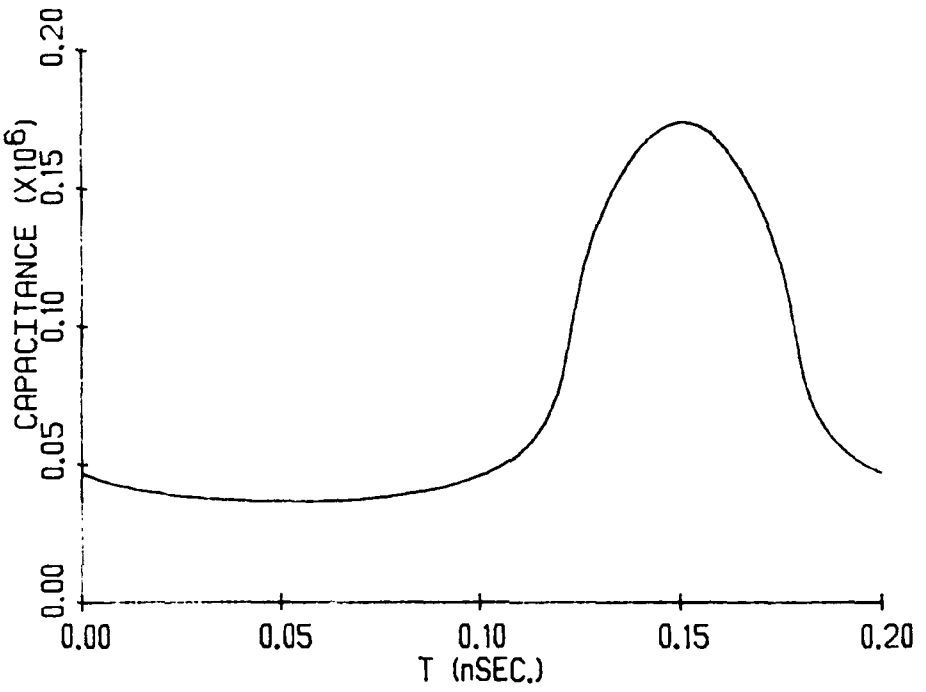


FIG. 19 CAPACITANCE/cm^2 FOR THE PROFILE IN FIG. 16 SUBJECTED TO THE VOLTAGE OF Fig. 18.

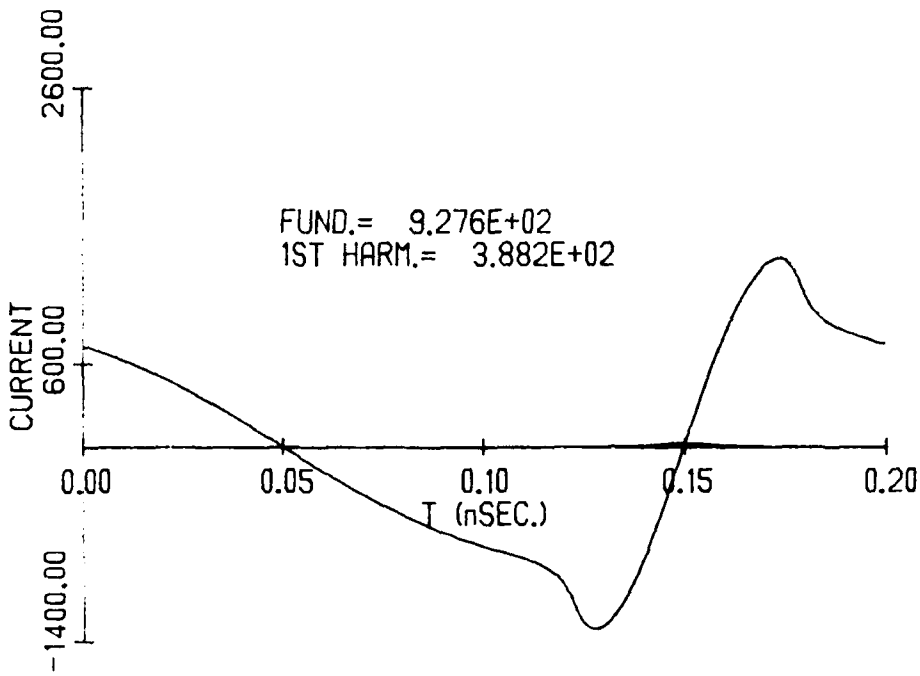


FIG. 20 CURRENT PRODUCED BY VOLTAGE AND CAPACITANCE WAVEFORMS OF FIGS. 18 AND 19. THE BARELY VISIBLE BUMP ON THE AXIS AT 0.15 ns IS THE NEGLIGIBLE CONTRIBUTION OF THE FORWARD-BIASED "DIODE" CURRENT.

to that of the MESFETs discussed previously with the exception of an etch that allows the ohmic contacts to be formed on the buried layer. The fabrication sequence is outlined in Table 1.

4.4.2 Monolithic Fabrication Sequence. The device structures discussed previously can be made monolithically compatible by selectively implanting a GaAs wafer with the desired profiles on different regions of the substrate. This can be done by masking the wafer with a dielectric layer and patterning this dielectric to create tubs of FET and varactor material on the substrate; by then using a mesa etch to isolate the devices, the lithographic requirements of the implantation are minimized.

If a methodology similar to that used to predict the doping profile in the substrate is used, the penetration of the dopant into the masking material can be calculated. In this case, however, the quantity of interest is the number of accelerated ions that will penetrate through a given thickness of the dielectric mask. Figure 11 shows a plot of this residual fluence for the varactor profile presented previously, where the material being considered is a silicon nitride mask layer. The effectiveness of a mask layer can be determined readily by such a plot. As an added safeguard, the isolation etch that is performed after the implants have been performed will remove any statistically insignificant number of dopant atoms that have managed to penetrate into the GaAs substrate. This process sequence allows for ease and process flexibility that is unavailable from other techniques. A brief outline of the complete fabrication sequence is given in Table 2.

Table 1

FET and Varactor Fabrication Steps

Process Step	FET	Varactor
Orientation etch	Deep etch performed on small portion of wafer to determine crystal orientation.	Same as FET.
Ohmic contact etch	Not required.	Etch through surface n-layer so contact can be made to buried n^+ layer. In situ determination of dopant concentration determined by probe-surface breakdown.
Ohmic contact formation	Ni-Ge-Au: 300 Å-400 Å-2800 Å. Alloy: 2 min at 490°C. Typical R_c = 1.5 x 10^{-6} Ω/cm^2.	Same as FET.
Mesa etch	$NH_4OH:H_2O:H_2O_2$ - 20:973:7 Etch rate ~ 33 Å/s. Probe-surface breakdown used to determine penetration through active layer.	Same as FET.
Schottky contact formation	Ti-Au: 700 Å - 2000 Å. Lithography schemes: AZ resist = ~0.75 μm resolution, poor liftoff, AZ resist with chlorobenzene = 1.5 μm resolution, good liftoff, AZ resist = w/Si_3N_4 ~0.75 μm resolution, good liftoff.	Same as FET.

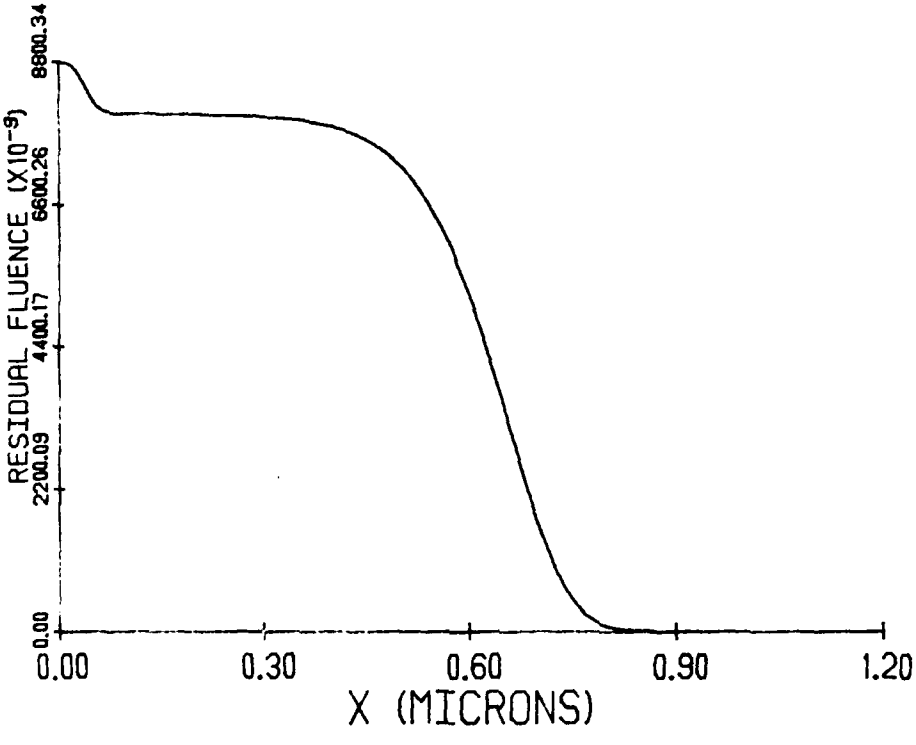


FIG. 21 RESIDUAL FLUENCE VS. DISTANCE INTO A Si_3N_4 SUBSTRATE FOR THE ENERGIES AND FLUENCES GIVEN IN FIG. 16.

Table 2

Monolithic Fabrication Sequence

Process Step	Process Description
Orientation etch and alignment marking	Deep etch performed on GaAs wafer to determine crystalline orientation and provide initial alignment reference.
Implant FET profile	Implant FET regions of wafer using Si_3N_4 mask.
Implant varactor profile and anneal	Implant varactor regions of wafer masking with Si_3N_4.
Varactor ohmic etch	Etch varactor ohmic pattern so contact can be made to n^+ buried layer.
Ohmic metallization	Ni-Ge-Au as described in Table 1 onto etched region for varactors and surface for FETs.
Isolation etch	As described in Table 1, but deep enough to isolate both FET and varactor profiles.
Schottky contact formation	Forms Schottky contact for both varactors and MESFETs as described in Table 1.
Lumped-element metallization	Forms interdigitated capacitors, loop inductors, or high impedance line sections; could be included with Schottky metallization for a well-developed process.

4.4.7 Conclusions. Monolithic fabrication of a harmonic power combiner was explored and appears to be a feasible method of extending the inherent power frequency limitations of a variety of solid-state active devices. GaAs MESFETs were fabricated and tested for use in this circuit. Varactor diode structures utilizing an ion implantation profile to produce enhanced harmonic generation capability were modeled and show promise as harmonic sources. Finally, a process sequence that makes these devices monolithically compatible was presented.

With these results in mind, monolithic fabrication of the doubler circuit should be feasible. Implementation of the circuit will require some developmental work on the most efficient configuration for the MESFETs as well as the evaluation of feedback capacitors and possibly loop inductors. These can probably be fabricated in a single-level metallization that has been provided for in the process sequence presented earlier. Once this circuit has been fabricated monolithically, the principles presented here should make the fabrication of higher-order combiner circuits feasible. This should allow for greatly improved performance from a variety of device structures.

SECTION V

MAGNETOSTATIC-WAVE DEVICE DESIGN AND ANALYSIS

The purpose of this phase of the program was to carry out a theoretical investigation concerning the magnetostatic modes of wave propagation in a magnetized YIG slab in a waveguide. An analysis was developed for a finite YIG slab and the properties of magnetostatic modes of wave propagation were obtained as a function of various parameters including the slab dimensions and its location in the waveguide structure as well as magnetic field.

The results obtained from the study were described in Technical Report No. AFWAL-TR-84-1174 entitled "Magnetostatic-Wave Propagation in a Finite YIG-Loaded Rectangular Waveguide," by M. Madhanesh, November 1984. The abstract of this report follows.

"The objective of this investigation is to study magnetostatic-wave propagation in a rectangular waveguide loaded with a finite YIG slab, to understand the effect of physical parameters on the dispersion and group time-delay characteristics, and to obtain better design criteria for magnetostatic-wave devices.

"An analysis was carried out for two basic geometrical configurations: (1) a YIG slab of arbitrary thickness placed inside a waveguide in contact with each sidewall and (2) a thin YIG slab of finite width placed symmetrically inside a waveguide such that there is an equal air gap between the slab and each sidewall. For each of these basic geometries, the magnetic bias field was assumed to be either parallel or normal to the slab in the transverse plane of

the waveguide. For Case 1, the mode analysis technique was used to obtain the dispersion relations while in Case 2 the integral equation method was used to derive the approximate dispersion relations.

"Numerical simulations were carried out for various geometrical configurations. Sample numerical calculations of the propagation constant and delay characteristics are presented in the frequency range of 4 to 10 GHz. These numerical results were obtained as a function of the geometry and magnetic field. The results obtained from the numerical simulation will be important in the design of magnetostatic-wave devices.

"The general formulation presented in this study contains all the information given by the degenerate cases previously published. The special cases of interest are obtained simply by permitting some of the dimensional parameters to take on their limiting values."

SECTION VI

CONCLUSIONS

Several important contributions were made during the course of this program. These were described in the body of the report as well as in detailed technical reports, journal articles and conference presentations. Significant contributions were made in the following areas:

1. Very comprehensive and excellent computer models were developed for IMPATT device simulations. These models were employed to compare with experimental results, where the agreement was found to be very good, and for optimum device design and prediction of the potential and capabilities of these devices for millimeter-wave power generation.

2. Both simple and approximate as well as comprehensive computer models were developed for GaAs MESFET simulation. These models were employed to determine small- and large-signal equivalent circuits for these devices and their dependence on material parameters and device geometry.

3. New measurement techniques were developed for characterizing FET devices and these techniques were employed to measure the small- and large-signal equivalent circuit parameters.

4. New ideas were developed and analyzed for power combining of two-terminal negative-resistance devices as well as three-terminal ones. A symmetrical fundamental and harmonic power-combining scheme

was developed that should be useful in extending the frequency of operation of solid-state devices.

5. The important elements, such as FETs and varactors that are needed for implementation of the symmetric power-combining scheme in a monolithic integrated circuit form, were fabricated and characterized.

6. A theoretical analysis was carried out on a finite YIG slab in a rectangular waveguide and for properties of the magnetostatic-wave propagation modes and their dependence on the YIG slab dimensions and its location as well as the magnetic field were determined.

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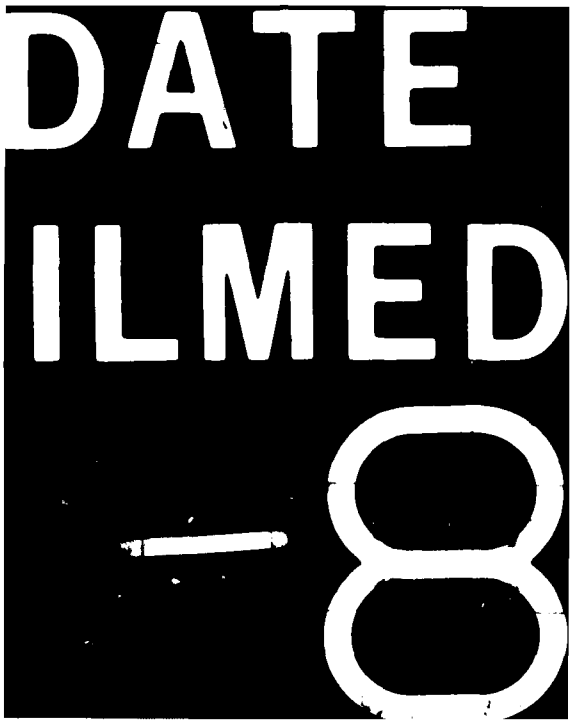
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